**Traffic Surveillance using global spatio-temporal technique**

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**121335001**

**Name of Guide: Dr. M.S.Sutaone**

Dynamic textures are temporally continuous and in-finitely varying sequences of images of moving scenes that exhibit certain spatial and temporal properties in time like sea-waves, smoke, foliage, whirlwind and have many potential applications. Such applications usually require dynamic texture segmentation that is not an easy task especially when the background is cluttered and textured. A new approach for segmenting a video sequence containing vigorous textures. The early method is based on a contourlet transform. This transform method agreed to re-evaluate spatio-temporal structures of a given scale and direction. This advances scrutinize and compare the scenario of the contourlet transform, a multiscale termination, for identify dynamic textures in image sequences and then intend a simple and efficient approach to dynamic texture segmentation using contourlet transform with measures to find the vibratory attribute. So that it is competent to specify the traffic of an image sequence by calculating the parameters.

The observation that, for objects that naturally move, it is frequently easier to identify them when they are moving than when they are stationary. But when there will be more traffic crowd that time very difficult to find the task features. The segmentation proficiency is well applied on video sequence of dynamic textures and also traffic classification has successful by measuring the density.

The outline of the research work summarized as chapters and subsections such as chapter I illustrates the dynamic texture properties. Chapter II is the study of literature cited. After that chapter III is spatio-temporal technique details as contourlet transform decomposition procedure. In chapter IV demonstrate proposed method. Chapter V is the explanation and implementation procedure and chapter VI is experimental results with modification and finally in chapter VII future prospects are finally discussed.

**Vehicle License Plate Detection and Character Recognition System on Raspberry Pi Board**

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**ABSTRACT**

With the increase in number of vehicles on road, traffic management is a recurring problem worldwide. This has led to the development of Intelligent Transportation System (ITS) with applications such as traffic management and law enforcement ,safety, real time monitoring of vehicles, theft detection of stolen vehicles and automatic ticketing at toll booths. License plate detection and recognition system (LPDR) plays a vital role in monitoring applications of ITS. The detection of the accurate location of a license plate is considered to be the most crucial step of LPDR system, which greatly affects the recognition rate and speed of the whole system. The character recognition is carried out after having the best plate candidate approved. The purpose of this project is to build hardware for offline system on Raspberry Pi which detects and recognizes license plates. The focus is on the design of algorithms used for extracting the license plate from a single image, isolating the characters of the plate and identifying the individual characters. Typically, an LPDR process consists of two main stages that are locating license plates and recognizing license plate characters. In the first stage, license-plate candidates are determined based on morphology based approach and Horizontal and vertical profile. The second stage comprises of character segmentation and recognition based on template matching method.

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MINIATURE INTEGRATED SEMICONDUCTOR BRIDGE CHIP FOR EXPLOSIVE INITIATON

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Name of Guide.: Mrs. P. P. Shingare

This report presents design of miniature integrated semiconductor chip

(SCB) for explosive initiation.The detonator has a microcontroller to detonate the

SCB chip. This circuit will use 6V for working and the dimensions are also minia-

turized to great extent. The circuit will provide lab programmability for setting

up delays for di\_erent applications. The trigger is provided for \_ring of SCB. A

6V supply voltage will be boosted to 50 Volts to charge Capacitor Discharge Unit

(CDU). After charging CDU to the desired voltage and after a preset delay, trigger

pulse will be given to turn on the electronic switch, and the SCB will \_re. The

circuit is programmable and all parameters like delays, trigger window and CDU

voltage can be controlled through software program. ESD and RF protection is

provided for safety.

**Memory Reuse Design for Low Power FPGA Systems**

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**Abstract**

Efficient utilization of memory resources is an ongoing process from beginning of FPGA systems. It is having highest priority for a system to fulfill all its necessary requirements with on chip resources rather depending on off chip resource.One of the main sources of system power consumption is external memory accesses, elements being repeated in nature cause most of memory being wasted, our approach is to take out only these elements and store them in local memories having limited sizethus we use data reuse approach to reducethe number of off-chip memory accesses.Multiple Choice Knapsack Problem (MCKP) plays an important role in our design where we end up having minimum weight and maximum profit. The experimental result show a verified power model under different scenarios and is capable to eliminate need of power hungry external sources, resulting in fast and efficient design methodology.

This design gives an exposure towards data reuse with help of MCKP which works in applications having repeatedly occurring data elements. We have made a two level memory design which takes runtime input sequence and it takes a decision on repetition of that element to store it on-chip or off-chip. We have used a single Block RAM for this design, inside which reuse arrays are mapped. However it can be made application specific for particular user, by increasing number of Block RAMs and hierarchy of reuse arrays. We get the reduced number of elements which we are storing on-chip after implementation of this design. This saves both power consumption and time factor of the processor as the numbers of iterations are reduced drastically. We can find accurate measure by increasing memory hierarchy of reuse arrays where we can focus on required data only. This design can be adopted for multimedia applications where repeatedly occurring data is processed at regular intervals. Image processing, ECG signal analysis are some domains where this method is very beneficial. Here we have shown results for distinguishing between 2D black and white images.

Automatic inspection method for solder paste Depositing

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**Abstract**

The Solder paste depositing inspection is very important in the process of Surface Mounting for print circuit board (PCB). An integrated inspection approach based on the machine vision was presented in the study. The method developed in this thesis can identify the major defects of the solder paste depositing, such as displacement, deficiency, excess, bridge and overflow.

Inspection of solder paste has been a critical process in the electronic manufacturing industry, to reduce manufacturing cost, improve yield, ensure product quality, reduce final faults and save rework cost. In this thesis, I am going to represent a computer vision system containing a stereoscopic camera, having inbuilt polarizing and diffusing illumination systems. Which help to provide us with an efficient solution for solder paste inspection. Our system uses a different technology to overcome some traditional technology approaches. I focus the less and excess amount of solder paste inspection occurs in the PCB. By using this technique, a solder paste is less or excess can be determined in percentage for circular and rectangular pad.

The solder paste inspection problem is more challenging than many other visual inspections because of the variability in the appearance of solder paste. Although many research works and various techniques have been developed to classify defect in solder paste, these methods have complex system of illumination for image acquisition and complicated classification algorithms. An important stage of the analysis is to select the right method for the classification. Better inspection technologies are needed to fill the gap between available inspection capabilities and industry systems.

Design Of Impedance Analyzer in 180nm Technology

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VLSI & EMBEDDED

ABSTRACT

This project presents a novel approach to estimate the impedance of a material/sample necessary in order to know its property and its behavior under various conditions. Using the fact that the permittivity of a dielectric mixture is proportional to its impedance, we validated our approach by making multi-frequency impedance measurements of a sample at different conditions and then comparing our results. The method provides a good estimate of knowing the factors affecting the property of material under certain conditions and it is applicable more generally in areas like soil moisture and ionic concentration detection, finding out strain of virus in blood sample, corrosion detection of material , non-destructive testing of a material etc. Digital approach is used in knowing the impedance of a material placed between electrodes from where a sine wave of known frequency and amplitude is passed from one electrode and the equivalent current is calculated and processed in the form of voltage by the application of amplifier from the second electrode .All simulations are done in the cadence virtuoso spectre simulator using libraries of gpdk 180nm and 90nm.

**Design High Performance 64-point FFT Processor for MIMO-OFDM**

Snehal Kalaskar

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VLSI & Embedded Systems

Guide: Mrs.Vanita Agarwal

**Abstract**

In recent years, as a result of advancing VLSI technology, OFDM has received a great deal of attention and been developed in many new generation wideband data communication systems such as IEEE 802,11A,digital audio/video broadcasting and in very high speed digital subscriber line (VDSL) in wired and wireless communications.FFT and IFFT are main arithmetic kernel in OFDM system.FFT are applied to OFDM System and it is implemented using VLSI design technique.

SIMULATION OF LOCOMOTIVE WAG9 SYSTEM

Ashwini A. Kulkarni

121335011

Name of Guide: Prof. Y.M.Vaidya

High fidelity simulation is commonly used for training drivers in the rail industry. There is need to improve the effectiveness of this training by making it adaptive to individual trainees and making use of the experiences on the field. The simulator is versatile enough to take care of training needs of not only the driving staff but also staff involved in maintenance and engineering development of locomotive. The WAG9 locomotive is GTO technology and microprocessor based train management and control system. The simulator allows training in individual high fidelity locomotive cab as well as in a multiuser/learner collaborative environment. The objective of transforming a passive trainee into an active, collaborative and participative member is achieved by allowing the trainee to interact with locomotive as well as the surrounding environment using 3D immersive gaming technology. The training strategy introduces the trainee at a base level and gradually increases the levels of complex systems in well planned multi loop adaptive learning strategy. This project outlines the features developed with each of the above in the mind seamlessly integrated into a versatile simulation training tool.

Chapter 1 gives a brief introduction of project outline, objective, challenges and outline of thesis.

Chapter 2 gives the literature review of the previous works in simulators, brief introduction of adaptive learning and WAG9 locomotive.

Chapter 3 discusses about the detailing for the design of work and implemented design.

Chapter 4 contains results and discussion in the form of figures.

Chapter 5 summarizes the work and concludes the project.

Keywords: Simulation based learning, 3D immersive environment, adaptive learning, Fidelity, Collaborative learning, locomotive, Simulation

**An Automated Fault Inspection System for PCBs**

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VLSI & Embedded Systems

Guide: Dr. Prashant P. Bartakke

**Abstract**

In electronics industry to communicate design information for the manufacturing of various types of printed circuits boards gerber format file is used. Manufacturing of PCBs is costly process so any defect during manufacturing should be avoided. Especially with the high level of complexity or many of today's boards. While printing film for bare PCB from photoplotter there may be improper printing of PCB film which further leads to production of defected PCBs. In this paper we are proposing a technique in which scanned image of bare PCB filmprinted from photoplotter and Image of PCB rendered from computer using gerber viewer toolare processed and from the results we can detect possible design faults or defects such as open tracks or shorts between two tracks. In proposed work we first apply image registration algorithm on both images to align them properly. Applying simple subtraction algorithm n both images and then thresholding subtraction result will highlight the defected region. Aim of the work is to detect defects in PCB film and finding defected area so that possible faults in PCB because of film can be avoided before PCB fabrication.

**Digital Video Stabilization**

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Guide: Dr. Prashant P. Bartakke

**Abstract**

Whenever video is taken from ordinary hand held mobile camera or camera mounted on vehicle (i.e. unstable platforms), video sequences captured suffer undesired motion as camera itself is vibrating. Hence, Videos captured by hand-held devices (e.g., cell-phones, portable camcorders or DVs) often look remarkably shaky. In this thesis we propose the algorithm for digital video stabilization to compensate camera motion.

Digital video stabilization is process of enhancing quality of shaky raw video by removing the undesired camera motions. It is image post processing.

Empirical evidence suggested that a simple global affine model for each pair of successive images followed by local integration of cumulative motion is sufficient for this purpose. It tracks Harris corners across frames and correlates this local information using algorithms like linear least squares to obtain a global motion model. Harris corners are tracked from frame to frame by template matching algorithm. As matching pairs are inliers data least square method is used to find geometric transformation.

**Tampering Detection and Localization using Digital Video Watermarking**

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Guide: Dr. S. P. Metkar

**Abstract**

Authentication is required to decide the originality of video signal. In this paper we proposed effective fragile video watermark embedding and extracting technique in DCT domain with high capacity and transparency. The bits of the digital signature of micro-block numbers and frame numbers are embedded as watermark in video frames in highest non-zero coefficient of quantized DCT coefficient. To ensure the authentication, along with the micro-block and frame number, the bits of digital signature of hash value are embedded into the frame as one of the watermark. This technique causes significantly smaller video distortion as bits are embedded into the highest frequency coefficients. The embedded watermark is extracted and verified using public key. The block numbers and frame numbers are inserted in order to detect intra-frame and inter-frame tampering such as addition or removal of content within frames, frame reordering, dropping or addition of extra frames. If the video is being tampered we may extract one watermark correctly but other may get destroyed. As a result tamper detection and authentication in videos is proved by digital watermarking.

Blind Watermarking for Depth Image Based

Rendering 3D Digital Video using SURF Algorithm

Sanket Kishor Mahajan

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Guide: Dr. S. P. Metkar

**Abstract**

Watermarking in 2D videos has already been explored in detail. Whereas nowadays 3D video is gaining more importance, so Research work is oriented more towards the 3D technology. There is a requirement of security measure to be considered for 3D content. There are several methods to secure 3D video. The depth-image-based rendering (DIBR) is one of the method used for watermark in 3D videos. DIBR method is very unusual and infrequently used in watermarking for 3D videos. With number of advantages, DIBR has became an important technology in 3D displaying, as a result, more and more copyright problems will turn out. DIBR 3D image is one of the image-based 3D data which consists of the center image and the depth image generated by the content provider. The left-eye image and the right-eye image are rendered from the center image and the depth image. We have proposed, novel watermarking technique is proposed to tackle with the security issues associated with DIBR 3D video. We used Speeded-up Robust Features (SURF) for finding the region where the watermark should be embedded. We used Improved Spread Spectrum (ISS) method to embed the watermark information into the DCT coefficients of the selected area. The experimental result shows, the proposed method is more robust to common signal distortion attack.

IMPLEMENTATION OF 128X64 BIT SRAM IN 90NM CMOS TECHNOLOGY

Neha Sant

MIS NO 121335016

Guide: Mr. P. P. tasgaonkar

ABSTRACT

This project focuses on design of 128x64 bit SRAM Block in 90nm CMOS Technology. The SRAM has row and column decoders, sense amplifiers, read/write circuitry and pre-charge circuit. This design aims to achieve minimum read static noise margin, minimize chip area and access time and maximum total power of 100 μWatts (leakage plus dynamic) both at nominal supply voltage of 1.2 Volts and worst case temperature of 110ºC. SRAM is designed using Cadence tool

**COMMUNICATION WITH POWER CONVERTERS**

Snehal R. Watharkar

MIS No-121335017

Guide: Dr. Prashant P. Bartakke

**Abstract**

This dissertation report presents various communication interfaces used to display electrical parameters and warning messages of power converters using RL78G14 microcontroller of Renesas make. Oriole Graphic Module 128x64 GLCD is used to display real time electrical parameters of single phase inverter. JHD 320x240 GLCD is used to display and control electrical parameters of Three phase Active filter and Static voltage regulator. GSM modem is used to send the fault and warning messages. USB protocol is used to download electrical parameters from power converters. SNMP card is used to monitor parameters through web access.

**Keywords: UART, GLCD module, RS232, SNMP protocol**

**Design of PFD, Charge pump and LPF for higher frequency PLL in 90nm CMOS Technology**

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For high speed communication(Gb/s), 57 to 64Ghz is very useful band. It is also challenging to design a circuit since, the circuit dimensions are comparable to wavelength. The Project involves the Design of Phase frequency detector, Charge pump circuit and Loop filter in 90nm CMOS Technology. Phase Frequency Detector is the digital components. Charge Pump and Low Pass Filter are the analog components. All components are designed and simulated on CADENCE tool (VIRTUOSO), whole design is optimized for minimum area. All components are integrated on chip, no off chip component is used. Loop Filter is the third order passive Low Pass Filter for better stability and Phase Frequency Detector is designed by using GDI cell having only 4 transistors with operating frequency of 5GHz . It has free dead zone. It can be used in high speed and low power consumption applications. This makes the proposed PFD more suitable to low jitter applications.Gate diffusion input (GDI)—a new technique of low-power digital combinatorial circuit design—is described. This technique allows reducing power consumption, propagation delay and area of digital circuits while maintaining low complexity of logic design. Charge Pump is used to convert phase difference signal to voltage signal and Divider is used to divide high frequency coming from oscillator. All circuits are simulated in Cadence Spectral.