E&Tc

College of Engineering, Pune

END SEMESTER EXAM

Year (S.Y. B.Tech, Spring 2011)

(ET-209)- (Microprocessors & Microcontrollers)

Day & Date-05/06/2011 Max. Marks-50

Timing-10am-1pm Duration -3 Hrs

Instructions:
1. Figures to the right indicate full marks.
2. All questions are compulsory.
3. Comments to the program is must.
4. Assume suitable data wherever needed.

Q1. Attempt the following. **(9)**

a) Discuss different data transfer schemes of microprocessor. **(3)**

b) Analyze the programme and find the contents of register A after execution of each step. **(3)**

```
MVI A, 07
RLC
MOV B,A
RLC
RLC
RLC
ORA A
```

c) Explain the importance of HOLD and HLDA pin data transfer through DMA. **(3)**

Q2 Attempt any three of the following. **(12)**

a) Explain Mode 0 of 8253 with appropriate timing diagram. **(4)**

b) What are the major limitations of 8085 interrupt scheme? How are the limitations overcome by 8259? Explain with the help of 8259 block diagram. **(4)**

c) What is MODEM? Explain the various MODEM signals. (with respect to 8257) **(4)**

d) What is the difference between a Timer and counter? Program Timer 0 to be an event counter. Use mode 2 and display the binary count on P2 continuously. Set the initial count to 20. **(4)**

Q3 **Attempt any three of the following.** **(15)**

a) Write a program for 8085 to find the sum of series 1-2+3-4+5-6+.....upto N terms. Assume nonzero value of N is available at memory location 2000H. Store the sum at 2001H. Write comments to the program. **(5)**

b) Assume XTAL= 11.0592 MHz. Write a program to generate a square wave of 50 Hz frequency on P2.3. Find the lowest frequency we can generate using Mode1. **(5)**

c) Program 8051 to receive bytes of data serially and put them in P1. Set the baud rate at 4800, 8-bit and 1 stop bit. **(5)**

d) Using 12 MHz crystal frequencies develop software to get continuous interrupts from Timer 0 after every 50 milliseconds continuously. **(5)**

e) Write a program to generate square wave of 1 KHz using counter 0. The clock of counter 0 is 1 MHz. The 8253 is connected in memory mapped I/O to generate address 8000H to 8003H. **(5)**

Q4 **Attempt any two of the following.** **(14)**

(a) Common anode seven segment display is to be interfaced to the 8051 µc. Give the interfacing diagram & write a program to display BCD digits 0 through 9 on seven segment display. **(7)**

(b) Design a memory system that provides 4 K EPROM immediately followed by 2 K RAM. EPROM implemented using 2732 (4k x 8) and RAM using (1K x 4). This memory system is interfaced with 8085 µp. Draw memory map & detail interfacing diagram. **(7)**

c) A peripheral device generates a low going pulse every time it has got a data byte ready for transfer. The device is interfaced with 8085 µp based system through 8255 connected in status check or polling I/O. Write a program that will transfer 100 bytes of data to µp & put it into memory starting from the location 3000H onwards. **(7)**

Data Given

8051

TCON:

D7							D0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TMOD:

D7							D0
G1	C/T	M1	M0	G0	C/T	M1	M0

SCON:

D7							D0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

PCON:

D7							D0
SMOD	....	.....	.....	GF1	GF0	PD	IDL

IE:

D7							D0
EA	x	ET2	ES	ET1	EX1	ET0	EX0

CWR: 8255

D7						D0
BSR/IO	Mode Selection	PORT A	PORT C_U	Mode Selection	PORT B	PORT C_L

Mode1: Status Word 8255

D7							D0
I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$

CWR: 8253

D7							D0
SC1	SCO	RW0	RW1	M2	M1	M0	BCD/Binary