COLLEGE OF ENGINEERING, PUNE

(An Autonomous Institute of Government of Maharashtra.)
SHIVAJI NAGAR, PUNE - 411 005

END SEMESTER EXAMINATION
(ET-203) Digital System Design

Course: B.Tech
Semester: III
Year: 2014-2015
Duration: 3 hrs

Branch: Electronics & Telecommunication
Max Marks: 60
Date: 26 NOV 2014
Time: 10am - 1pm
MIS no:

Instructions:

1. Figures to the right indicate the full marks.
2. Mobile phones and programmable calculators are strictly prohibited.
3. Writing anything on question paper is not allowed.
4. Exchange/Sharing of anything like stationery, calculator is not allowed.
5. Assume suitable data if necessary.
6. Write your MIS Number on Question Paper

Q.1 Solve the following (any five) (10)

a) Express the decimal numbers into Gray and 2421 code
   1) 547 2) 221

b) Simplify using Boolean algebra
   $AB + \overline{AC} + A\overline{B}C(AB + C)$

c) Without simplification, implement f (w, x, y, z) = Σ m (0 2 5 7 13 15) using only 2:1 MUX. Use as many as you need

d) Convert T FF to D FF

e) Explain the hazards in combinational circuits

f) Explain the terms : Entity and architecture

Q.2 a) Design a system for a car to be started based upon whether a passenger is present and whether both passenger and driver have their seat belts on. Use best suitable MSI device for implementation. (5)

b) Design a 8:3 priority encoder that resolves priority among eight active high inputs I0-I7, where I7 has the highest priority. The circuit should produce an output to indicate the number of the highest priority enabled input. If no input is enabled then output should be=111. (5)

Q.3 A clocked synchronous sequential circuit using positive edge triggered D FFs has an input x and output Z. The excitation equations are: $Y_1 = y_1.\overline{x} + y_0.x$

$$Y_0 = y_0.\overline{x} + \overline{y_0}.x$$

$$Z = y_1.y_0.x$$

Obtain the logic diagram, state diagram and state table, also redesign the circuit using J-K FF. (10)

Q.4 a) Implement the following functions using 3x4x2 PLA (3i/p,4 products & 2 outputs)
   F_1 (A,B,C)= Σm(3,5,6,7) and F_2(A,B,C)=Σm(0,2,4,7) (5)

b) How does a totem-pole gate differ from an open collector gate? (5)

Q.5 a) Assume you have an 8-bit ALU which executes 4 functions: addition when the control input is 00, subtraction when the control input is 01, AND when the control input is 10,and OR when the control input is 11. Write a VHDL description whose behavior is the same as the above mentioned ALU (8)

b) Write down the value of S1, S2 and S3 for the first three clock cycles (2)

```
signal S1, S2, CLK: BIT:='0';
begin
process (clk)
variableV1: BIT: = '0';
begin
V1 := not V1;
S1  <= V1;
S2  <= S1;
end process;
```

Q.6 Explain the terms with neat diagrams (any two) (10)

1. Source current and sink current
2. Fan in and Fan out
3. I/P and O/P profile of TTL
4. Interfacing TTL and CMOS