E&TC

College of Engineering, Pune

END SEMESTER EXAM

(T.Y B.Tech)

(ET 303- COMPUTER ORGANISATION & ADVANCED MICROPROCESSORS)

Day & Date-Tuesday-30/11 /2012 Max. Marks-50

Timing- 2.00 to 5.00 p.m Duration 3 hrs

Instructions:

1.All Questions are Compulsary.
2.Draw neat Diagram wherever necessary.
3.Figure to the right indicate full marks.
4. All the variables have their usual meaning.

Q. 1 A. Multiply the given pair of signed 2's complement number , (5)

Multiplicand - A, Multiplier - B

i) A:10101101, B: 10101011 Using **Booth's Algorithm**

ii) A: 01110101, B: 10001011 Using **Bit Pair recoding**

B. What are the three schemes that can handle more than one interrupting device? (3)

Q.2 A. State the functions of I/O Interface circuit? (2)

B. For an 8-bit input port, what are the steps for connection between keyboard and the processor. (4)

OR

B. Draw and explain the two ways of arbitration in DMA to resolve the conflicts of the devices for using the system bus. (4)

C. Explain the data transfer of asynchronous bus for an input operation using the timing diagram. (4)

Q. 3 A. How the Cache memory acts as a faster memory to the processor? (3)

B. What are the different mapping techniques of the cache memory? (3)

C. Explain in brief about the construction and working principle of the magnetic hard disk. (6)

Q. 4 A. With a neat diagram, Describe the functions of system segment and gate descriptors format. (4)

B. Justify your answer with a proper diagram why the interleaved multithreading is better than blocked multithreading? What are the commercial multithread processors. (5)

C. Calculate latency (w) in the blocked multithreading ; (1)

Given: p = 9 , n=3, q= 1

Q.5 A. Draw a flowchart for the program given below. (1)

B. Write an assembly language program using 8086 instructions and directives to find the **factorials** of numbers from 01 to 07H that are present from the **DATA** segment offset of 2500H and store the result (**factorials**) from the **EXTRA** segment offset of 0500H onwards. (4)

C. Draw and Explain the hardware platform for the design of Multi-Radio Communications Gateway with the context of Intel ATOM E6XX series processor. (5)

-x-x-x-x-x-x-x--