COLLEGE OF ENGINEERING, PUNE

(An Autonomous Institute of Govt. of Maharashtra)

END-SEM EXAM

Computer Organization

Program: T.Y.B. Tech (Computer Engineering)

Year: 2013-14 Semester I November 2013

Duration: 3 hrs Max. Marks: 100

Instructions:

1. Answer all questions.
2. Figures to right indicate full marks
3. Draw neat figures wherever required.
4. Assume suitable data, if necessary.

Marks

Q.1 Consider the following part of code for adding vector **A** and a vector **B** , storing the result back to vector **A**.

```
#define N 4096
int A[N], B[N];
int i;
.
.
for(i = 0; i < N; i++)
A[i] = A[i] + B[i];
.
.
```

Assume that in the system the main memory address is 32 bits and having two-way set-associative cache with 16 bytes per block, set field of 8bits and having LRU replacement policy. Initially cache is empty.
Also assume **A** and **B** are cache aligned to a 4KB boundary and are contiguous in main memory.
integers are 32 bits.

i) What is the miss-rate for the two-way set-associative cache for running the above for_loop code? 7

ii) What is the Average Memory Access Time for running the above for_loop code for the two-way set-associative cache? Assume hit time 1 cycle & the miss penalty is 20 cycles. 3

b Explain double precision IEEE754 standard for floating-point number representation and the ranges of numbers getting represented therein. 6

P.T.O.

Q.2	a	Show the organization of a single bus CPU having eight general purpose registers R0, R1, ... R7 & required dedicated registers along with other functional blocks. What are the control signals to be generated for executing the instruction ADD4RGS; to add contents of four registers R1, R2, R3 & R4 and storing the result in memory pointed by R5	**10**
	OR		
	a	Explain the loading of Disk Operating System along with the memory map.	**10**
	b	What is the lookahead carry in four bit addition?	**6**
Q.3	a	Apply both, the Booth recoding Technique & Bit pairing Technique for each of the following Multiplication: i) 13 x 7 ii) 19 x -5	**12**
	b	Give the lower 1MB memory map of x86 based computing machine.	**6**
Q.4		Describe the MBR hard disk and GPT hard disk	**18**
Q.5	a	What are the techniques for Bus Arbitration in multiprocessor system?	**12**
	OR		
	a	What are the characteristics and patterns of instruction execution encouraging for design of RISC? What are the characteristic of RISC?	**12**
	b	What are the instruction encoding formats of instruction meant for NDP 8087?	**4**
Q.6		Answer the following	**16**
	a	What is the purpose of Tag Bits in NDP 8087?	
	b	What will be the dot clock rate for monochrome display adapter for displaying 25 information lines of text with 100 characters per line, assuming the character dot matrix size of 8 columns & 8 rows (8x8)?	
	c	What is the role of page table in translation of virtual address to physical address?	
	d	What is the bottleneck in using RAID 4 (Block level parity) hard disks and how is it avoided with other appropriate RAID Level?	