College of Engineering, Pune

End Semester Examination

T. Y. Electrical Engineering

EE 009002: Microcontroller

Date: 13/11/2013 Time: 2.00 to 5.00 pm
Day: Wednesday Marks: 60
Instructions:

1. All the questions are compulsory.
2. Assume suitable data wherever necessary.
3. All the questions carry equal marks.
4. Figures to the right indicate full marks.

Q.1A) Find the on-chip program ROM size in K for the AVR chip with the following address ranges: [5 M]
(a) $0000-$1FFF (b) $0000-$3FFF (c) $0000-$7FFF (d) $0000-$FFFF
(e) $0000-$1FFFF (f) $00000-$3FFFF (g) $00000-$FFF (h) $00000-$1FF
Based on which criteria, you will select a specific microcontroller for particular microcontroller?

Q.1B) Write an assembly program for a nested loop to perform an action 100,000 times. [5 M]

Q.2A) Write an assembly program to monitor PB4. When it goes HIGH, the program will generate a square wave of 50% duty cycle on pin PB7. [5 M]

Q.2B) Why do we use the code space for video game characters and shapes? What is the advantage of using code space for data? What is the drawback of using program code space for data? [5 M]

Q.3A) Program Timer0 in C to generate a square wave of 3KHz. Assume that XTAL = 16 MHz. [5 M]

Q.3B) Explain what happens if both INT1F and INT2F are activated at the same time. [5 M]

Q.4A) Write an AVR C program to transmit serially the message "The earth is but one country and mankind its citizens" continuously at 57,600 baud rate. [5 M]

Q.4B) There are two methods of sending commands and data to the LCD: (1) 4 bit mode or (2) 8 bit mode. Explain the difference and advantages and disadvantages of each method. [5 M]

Q.5A) In the A/D of ATmega32, what happens to the converted analog data? How do [5 M]

we know that the ADC is ready to give us the data? What happens to the old data if we start conversion again before we pick up the last data?

Q.5B) What are different types of relays? Where will you use them? Design an application where relay can be used along with microcontroller. [5 M]

Q.6A) Using Timer0, no prescaler and CTC mode, write a program that generates a square wave with a frequency of 80 KHz. Assume XTAL = 8 MHz. [5 M]

Q.6B) Using Timer0 and non inverted Fast PWM mode, write a program that generates a wave with frequency of 62.5 KHz and duty cycle of 60%. Assume XTAL = 16 MHz. [5 M]

Table 11-4: UBRR Values for Various Baud Rates (Fosc = 8 MHz, U2X = 0)

Baud Rate	UBRR (Decimal Value)	UBRR (Hex Value)
38400	12	C
19200	25	19
9600	51	33
4800	103	67
2400	207	CF
1200	415	19F

Note: For Fosc = 8 MHz we have UBRR = (500000/BaudRate) – 1

UCSRA Register:

RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM

UCSRB Register:

RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM

UCSRC Register:

URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL

Bit	7	6	5	4	3	2	1	0
	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00
Read/Write	W	RW	RW	RW	RW	RW	RW	RW
Initial Value	0	0	0	0	0	0	0	0

FOC0 D7 Force compare match: it is a write-only bit, which can be used while generating a wave. Writing 1 to it causes the wave generator to act as if a compare match has occurred (see Chapter 15).

WGM01:00 D3D6 Timer0 mode selector bit

0 0	Normal
0 1	PWM, Phase correct
1 0	CTC (Clear Timer on Compare match)
1 1	Fast PWM

COM01:00 D5 D4 Compare Output Mode when Timer0 is in Fast PWM mode

COM01	COM00	Mode Name	Description
0	0	Disconnected	Normal port operation, OC0 disconnected
0	1	Reserved	Reserved
1	0	Non-inverted	Clear OC0 on compare match, set OC0 at TOP
1	1	Inverted PWM	Set OC0 on compare match, clear OC0 at TOP

CS02:00 D2D1D0 Timer0 clock selector

0 0 0	No clock source (Timer/Counter stopped)
0 0 1	clk (no prescaling)
0 1 0	clk / 8
0 1 1	clk / 64
1 0 0	clk / 256
1 0 1	clk / 1024
1 1 0	External clock source on T0 pin. Clock on falling edge
1 1 1	External clock source on T0 pin. Clock on rising edge

Figure 16-12. TCCR0 (Timer/Counter Control Register) Register