Computer

# College of Engineering, Pune - 05
# End Semester Exam – November 2012

## Final Year B. Tech. (Computer Engineering)
## (CT-404) Advanced Computer Architecture

**Duration** – 03 Hrs. **Maximum Marks:** 100
**Date:** 27th November 2012

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**Instructions:**

1. Figures to right indicate full marks.
2. Draw neat diagrams at appropriate places.
3. Assume suitable data wherever necessary and state appropriately.

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Q. 1 **Solve the following.** 20

A. What is instruction level parallelism? Discuss the limitations of instruction level parallelism.

B. What is the role of branch target buffer in dynamic branch prediction?

C. What is the serious problem given by fixed load speedup model? How it can be removed?

D. Which buffers do we use in prefetch buffer mechanism? What is difference between sequential buffer and target buffer?

E.
   a. Let x= (2, 5, 8, 7) and y= (9, 3, 6, 4). What result it will yield if we use compare instruction?
   b. Let x= (1, 2, 3, 4, 5, 6, 7, 8) and y= (1, 0, 1, 0, 1, 0, 1, 0). What result it will yield if we use compress instruction?
   c. Let x= (1, 2, 4, 8), y= (3, 5, 6, 7) and B= (1, 1, 0, 1, 0, 0, 0, 1). What result it will yield if we use merge instruction?

F. Which are the parameters that characterize a SIMD computer?

G. Let $\alpha$ be the percentage of a program code which can be executed simultaneously by n processors in computer system. Assume that the remaining code must be executed sequentially by a single processor. Each processor has a execution rate of x MIPS and all other processors are assumed equally capable.
   a. Derive an expression for the effective MIPS rate when using a system for exclusive execution of this program, in terms of the parameters n, $\alpha$, x.
   b. If n=16 and x=400 MIPS, determine the value of $\alpha$ which will yield a system performance of 5000 MIPS.

H. Which are the reasons that causes inconsistencies in cache?

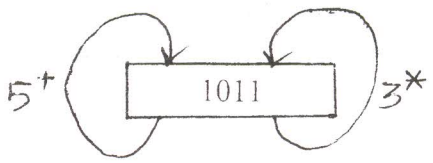
I. Discuss processor characteristics for multiprocessing.

J. Differentiate between synchronous and asynchronous message passing.

Q. 2 A. List different latency hiding techniques. Briefly explain the prefetching technique along with its advantages. 8

B. Discuss Tomasulo's algorithm for dynamic instruction scheduling. 4

C. Consider the following state transition diagram with MAL=3. How can we reduce the MAL by inserting delays? 8




Q. 3 A. For following sequence of four vector instructions, explain the process of pipeline chaining. 8

$V_0 \leftarrow$ Memory (Memory Fetch)
$V_2 \leftarrow V_0 + V_1$ (Vector Add)
$V_3 \leftarrow V_2 < A_3$ (Left Shift)
$V_5 \leftarrow V_3 \wedge V_4$ (Logical Product)

B. Which are the problems of asynchrony? How does the distributed caching overcome this problem? 8

C. Explain parallelism profile in a program. 4

Q. 4 A. Explain shared-memory model. What do you mean by incremental parallelism? How shared-memory model differs from message passing model? 8

B. Write down basic concept of directory based cache coherence scheme. List the states in full mapped directories with diagrams. Which is the overhead associated with full mapped directories? 8

C. Discuss a cube interconnection network for SIMD architecture. 4

Q. 5 A. What do you mean by a communicative group? Discuss collective operations in MPI. 8

B. Discuss the cache coherence problem. How does the Snoopy bus protocol ensure the coherence? 8

C. Explain working of OpenMP standard. 4