E&TC

COLLEGE OF ENGINEERING, PUNE-5.

(An Autonomous Institute of Government of Maharashtra)

END SEMISTER EXAMINATION (2012-2013)

Total No of Questions: 5 Total No of Pages:2

Final Year B.Tech. (Electronics and Telecommunication)

Subject: (ET411-2)Elective: RISC Microcontrollers and DSP Processors

[Time: 3 Hours] **[Max. Marks: 50]**
Year: 2012-13 (November 2012)

Instructions to candidates:
1) All questions compulsory. 2) Neat Diagrams must be drawn wherever necessary.
3) Assume suitable data if necessary. 4) Figures to the right indicate full marks.
5) Use of non-programmable electronic calculator is allowed.

Q.1	(a)	How efficiency of Reduced Instruction Set Computer is increased by instruction pipelining? Illustrate with four stage pipeline.	4
	(b)	Specify and elaborate following issues the designer should handle when porting the C code onto ARM platform. i) Inline assembly ii) The volatile keyword	3
	(c)	Draw a typical AMBA –based microcontroller system. What are the significant feature implemented in AMBA AHB for high performance, high clock frequency systems?	3
Q.2	(a)	Present the scheme in detail of a prioritized simple interrupt handler handling prioritized interrupts on ARM processor.	4
	(b)	Write a C code to divide 32 bit unsigned number by another 32 bit unsigned number. Write complied assembly code for above C program. If divisor needs to be used several times, how can the process of division be optimized? Justify the same with suitable mathematical analysis.	6

Q.3 Illustrate the processor operations using examples with pre and post conditions, describing registers and memory before and after the instructions are executed. **10**

i)STMED sp!,{r1,r2}

ii) SMLATB r4,r1,r2,r3

iii)MPYHL.M1 A4,A5,A6

iv)LDW.D1*A0++[2],A1

v)MVK.S1 0X1223,A1

Q.4(a) Present the details of following special addressing modes that permit single word/instruction format and thereby speed up the execution in P-DSPs. **5**

i)Memory –mapped Addressing

ii)Indirect Addressing

iii) Bit Reversed Addressing mode

(b) Write assembly code in TMS320C6x processor for convolution of two sequences x(n),h(m) of length N and M respectively. **5**

For N=7 and M=5 and x(n), h(m) are given by

x(n)=1, 2, 2,2,2,2,1 where $0 \leq n \leq 6$

h(m)= 1,2,2,2,1 where $0 \leq m \leq 4$

Q.5(a) Name different units in the central processing unit of 'C6x device and draw the various fields of Control Status Register (CSR) of 'C6x. **5**

Write functions of fields SAT,PCC,GIE and Revision ID in CSR.

(b) Discuss various steps involved to achieve design of FPGA based systems with the help of CAD tools. **5**

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