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COLLEGE OF ENGINEERING, PUNE

(An Autonomous Institute of Govt. of Maharashtra)

Final Exam 2013

(CT 404) Advanced Computer Architecture

Class: - B.Tech (Computer Engineering)

Year: - 2013-14 **Semester: - VII**

Duration: - 3 hr **Max. Marks: - 60**

Instructions:

1. **All the Questions are compulsory.**
2. **Assume suitable data whenever necessary.**
3. **Draw neat figures wherever required**
4. **Figures to right indicate full marks**

Q. 1 Multiple Choice Questions (MCQs) **10**

1. Itanium processor: Which hazard can be circumvented by register rotation
   a. Control Hazards
   b. Data Hazards
   c. Structural Hazards
   d. None
   e. None of the answer above is correct.
2. Interconnection network, topology :How many links has a 5 by 5 mesh?
   a. 16
   b. 25
   c. 40
   d. 50
   e. None of the answer above is correct
3. The hardware mechanism that enables a device to notify the CPU is called_____.
   a. Polling
   b. Interrupt
   c. System Call
   d. None of the above
4. An interrupt for which hardware automatically transfers the program to a specific memory location is known as
   a. Software interrupt
   b. Hardware interrupt
   c. Maskable interrupt
   d. Vector interrupt
5. In register stack a stack can be organized by a _____number of register:
   a. Infinite number
   b. Finite number
   c. Both
   d. None
6. Instruction formats contains the memory address of the_____:
   a. Memory data
   b. Main memory
   c. CPU
   d. ALU
7. Address format can be represented as :
   a. dst <-[src1][src2]
   b. dst ->[src1][src2]
   c. dst <->[src1][src2]

d. All of these

8. In which addressing the operand is actually present in instruction:
   a. Immediate addressing
   b. Direct addressing
   c. Register addressing
   d. None of these
9. length instruction some programs wants a complex instruction set containing more instruction, more addressing modes and greater address rang, as in case of_____:
   a. RISC
   b. CISC
   c. Both
   d. None
10. which instruction are used to perform Boolean operation on non-numerical data:
   a. Logical and bit manipulation
   b. Shift manipulation
   c. Circular manipulation
   d. None of these

Q. 2 Write down True or False: 5

1. Computations need not to be completed within a "reasonable" time period
2. Given p processors and f the maximum fraction of a problem that can be provided into parallel tasks, Amdahl's law predicts that as p goes to infinity, the speedup S(p) approaches 1/f.
3. Linear Speedup is defined as maximum speedup is usually p with p processors.
4. Parallel computing is using more than one computer, or a computer with more than one processor, to solve a problem.
5. Mutual Exclusion is a mechanism for ensuring that only one process accesses a particular resource at a time to establish sections of code involving the resource as so-called critical sections and arrange that only one such critical section is executed at at time.

Q. 3 Fill in the blanks: 5

1. A _____ process is a process that is treated as a completely separate program with its own variables, stack, and memory allocation.
2. _____ are groups of interconnected "commodity" computers achieving high performance with low cost.
3. _____as a parallel programming platform is an alternative to expensive supercomputers.
4. A hardware design that allows the system to be increased in size and doing so to obtain performance could be described as _____ or _____.
5. Loosely coupled is also called as_____.

Q. 4 What is Latency hiding technique? Elaborate with example. 8

Q. 5 Discuss the various context switching policies implemented in multithreading architecture. 4

OR

Suppose the time delay of the four stages are τ_1=40ns, τ_2=90ns, τ_3=70ns, τ_4=80ns and the interface latency has a delay of τ_l=12ns. Calculate cycle time, clock frequency, speedup over the non-pipeline adder design and maximum speedup

can be achieved.

Q. 6	What is the difference between grid computing and cluster computing? Discuss features of grid computing.	8
Q. 7	Explain with diagram COW and NOW architecture.	5
Q. 8	Explain in brief the programming model of Cray-1 vector processor.	8
Q. 9	Explain the architecture of itaniun processor in details.	7