COLLEGE OF ENGINEERING, PUNE

(An Autonomous Institute of Government of Maharashtra.)
SHIVAJI NAGAR, PUNE - 411 005

END SEMESTER EXAMINATION
ET (DE)- 14004 RISC Microcontrollers and DSP Processors

Course: B.Tech.
Branch: Electronics & Telecommunication Engineering
Semester: VII
Year: 2014-2015
Max Marks: 60
Date: Nov 2014 28 NOV 2014
Duration: 3 Hours
Time: 2 to 5 p.m.
MIS no:

Instructions:

1. Figures to the right indicate the full marks.
2. Mobile phones and programmable calculators are strictly prohibited.
3. Writing anything on question paper is not allowed.
4. Exchange/Sharing of anything likes stationery, calculator is not allowed.
5. Assume suitable data if necessary.
6. Write your MIS Number on Question Paper
7. Draw neat diagrams wherever necessary.
8. All questions are compulsory.

Q.1 (a) How instruction pipelining improve throughput in P-DSPs? Explain the approach with the help of pipeline having depth of four. **(5)**

(b) Name various special addressing modes in P-DSPs and explain Short Immediate and Memory-mapped addressing modes in details. **(5)**

Q.2 (a) The functional units in the following instruction are missing. List the same and explain your answer for 'C6X DSP processor family **(6)**

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[B1] B ??? LOOP
LDW ??? *+A0[1],A1
MPY ??? B2,A1,B4
ADD ??? A0,B1,A2
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(b) You are given (x,y) coordinates of two points as (4,4) and (12,12) respectively. Using TMS320C6713 DSP processor instruction set, develop an assembly code to compute Euclidian distance between the two points. **(4)**

Q.3 (a) How various operations are simplified by BIT-BAND operation in the Cortex-M3 processor? Explain. **(4)**

(b) With the help of example showing contents of registers, SP,LR, memory, special registers before and after execution. Explain following instructions in Cortex-M3. **(6)**

(i) MOV R1,# 'G'
(ii) LDRH Rd,[Rn, #offset]
(iii) ANDS R0,R0,R1
(iv) STMIA .W R8!,{R0-R3}
(v) BL Print Text

Q.4 (a) State functions carried by PRIMASK, FAULTMASK and BASEPRI Registers used to disable exceptions in Cortex-M3. **(6)**

(b) Justify the necessity of the Two-Stack Model in Cortex-M3. **(4)**

Q.5 (a) Write and Explain C Program to send text message "Good Afternoon" to a consol through the UART in the Cortex-M3. **(6)**

(b) Explain how Memory management faults are handled by various system exceptions in the Cortex-M3 **(4)**

Q.6 (a) Explain the functions carried by Program fetch unit, Instruction dispatch unit and Instruction decode unit in the Central Processing Unit of 'C6X device. **(5)**

(b) What is Fuzzification and Defuzzification in a fuzzy logic based Embedded Controllers? **(5)**

OR

(b) Differentiate between-

(i) Fuzziness and Probability

(ii) Fuzzy Logic and Multiple-Valued Logic

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