COLLEGE OF ENGINEERING, PUNE

(An Autonomous Institute of Government of Maharashtra.)
SHIVAJI NAGAR, PUNE - 411 005

END Semester Examination

(CT(DE)-14006)   High Performance Computing

Course: B.Tech   Branch: Information Technology

Semester: Sem VII

Year: 2014-2015   Max.Marks:60

Duration: 3 Hours   Time:- 2 to 5 p.m   Date: 8 NOV 2014

Instructions: MIS No. ☐☐☐☐☐☐☐☐ ☐

1. Figures to the right indicate the full marks.
2. Mobile phones and programmable calculators are strictly prohibited.
3. Writing anything on question paper is not allowed.
4. Exchange/Sharing of anything like stationery, calculator is not allowed.
5. Assume suitable data if necessary.
6. Write your MIS Number on Question Paper

Q. 1   **Solve the following.**

A.   You have a choice between two processors. The first processor is a single core that can operate at 2 GHz at 1.13V. The second processor is a dual core version of the first processor. It operates at 1.2 GHz at 1V (two cores). Which processor would you use for a mixed (equal sections of serial and parallel code) workload where low power consumption is of the utmost importance?   [3]

B.   What memory architecture would you suggest for a multiprocessor system that consists of a single motherboard, with 4 processor chips, each chip being an 8 core processor (Total 32 cores on one board)? All memory will be connected to this single board. Justify your answer.   [3]

C.   Draw the CPU-cache state transition diagram for a bus based snooping cache coherence system. Label each transition clearly and explain each action and the bus actions it generates.   [5]

Q. 2   **Solve the following.**

A.   Explain the benefits of a Load Linked/Store Conditional pair over a Test and Test and Set lock. Is the LL/SC pair atomic?   [2]

B.   List the 3 types of pipeline hazards and explain them briefly.   [3]

C. You have a system where 3 threads are running, time sliced by the operating system. This is being run on a single core, single thread processor that can work on 4 instructions in one cycle. Look at the following schedule table. Time increases as we go down. Each instruction is labelled with its thread (A/B/C), and it's earliest execution time with respect to the start of the thread. Schedule this for a 4-wide processor that supports SMT4. What is the new time for execution?

T				
0	A0	A0	A0	
1	A1			
2	A2	A2		
3	A3	A3	A3	
4	B0			
5	B1			
6	B2	B2	B2	B2
7	B3	B3		
8	C0			
9	C1	C1	C1	C1
10	C2			
11	C3	C3	C3	

[3]

D. The following instruction trace runs on a dual core processor, with two cores, labelled C0 and C1. Show all the core side requests and bus actions for each core after each request. Assume each distinct address is in a different cache line.

Instruction	Core0	Core1
Ld0 R1, A		
Ld1 R1, B		
Ld0 R2, B		
St0 A, R4		
St1 B, R6		
Ld0 R3, A		
Ld0 R8, B		
St1 B, R9		

[4]

Q. 3 **Solve the following.**

A. Compare performance of two CPUs

- CPU with ideal memory, no cache misses
  Average one clock per instruction
  Cycle time is 1 ns
- CPU with real memory, cache misses occur
  Similar to above, plus
  60% of instructions are loads/stores (mem accesses)
  4.7% of accesses miss cache
  18 cycle miss penalty

[4]

B. Calculate the size of a G Select branch predictor that uses 9 bits of the instruction address to index into the BHT. Each entry in the BHT uses a 2 bit smith counter to make a prediction. The GShare predictor uses 4 bits of history. Ignore the size of the history register. Assume 32 bit addresses. [3]

C. Discuss asynchronous and synchronous message passing methods. [3]

Q. 4 **Solve the following.**

A. For following sequence of four vector instructions, explain the process of pipeline chaining. [5]
V_0 Memory   (Memory Fetch)
V_2 $V_0 + V_1$ (Vector Add)
V_3 $V_2 < A_3$ (Left Shift)
V_5 $V_3 \wedge V_4$ (Logical Product)

B. Let X=(2, 5, 8, 7) and Y=(9, 3, 6, 4). Apply compare instruction B=X > Y
Let X=(1, 2, 4, 8),Y=(3, 5, 6, 7) and B=(1, 1, 0, 1, 1, 0, 0, 1). Apply merge instruction. [2]

C. Differentiate between CPU and GPU. Explain GPU architecture. [5]

Q. 5 **Solve the following.**

A. Explain the working of message passing interface along with gather scatter operations. [5]

B. Discuss steps involved in building MPI cluster. [5]

C. Which are the factors that affect design space of interconnection networks? Explain different interconnection networks used in SIMD architectures. [5]