ELECTRONICS & TELECOMMUNICATION ENGINEERING

M.Tech.(Electronics-VLSI and Embedded Systems)

Effective from A. Y. 2011-12

INDEX

List of Abbreviations

Sr. No.	Abbreviation	Stands for:
1	DEC	Departmental Elective Course
2	PCC	Program Core Course
3	LC	Laboratory Course
4	HSSC	Humanities and Social Science Course
5	MLC	Mandatory Learning Course
6	LLC	Liberal Learning Course
7	OEC	Open Elective Course
8	SEC	Science Elective Course
9	PSEC	Program Specific Elective Courses

M. Tech., RULES AND REGULATIONS
(Effective from 2011-12)

COLLEGE OF ENGINEERING, PUNE
Wellesley Road, Shivajinagar, Pune 411005

1. Rules

1.1 The Senate and BOG, College of Engineering, Pune, recommends University of Pune to award the degree of Master of Technology (M. Tech) in Engineering to those who have successfully completed the stipulated Postgraduate Masters Program.

1.2 The Postgraduate Masters Program with the governing Rules and Regulations are formulated & approved by the Senate and BOG of the institute. The Senate can modify or change the course structure, the governing rules and regulations from time to time and shall recommend them to BOG for its approval. These rules and regulations will be applicable to any candidate seeking admission for M. Tech/P.G. programme in the institute.

1.3 A candidate becomes eligible for the recommendation to the Pune University for the award of the M. Tech. degree after fulfilling all the academic requirements prescribed by the Senate of the Institute.

1.4 Director, COEP and Chairman Senate would appoint a Professor from the Institute to work as a Chairman of the PG admission committee on his/behalf. Chairman, PG Admissions would be responsible for the entire admission process including scrutiny of applications and conduct of entrance test, interviews of the candidates etc. He/she would be assisted by the respective departmental heads and departmental admission committee appointed by the Director.

2. CATEGORIES OF M. TECH. STUDENTS

The Institute admits M. Tech students under the following categories:

I) REGULAR (FULL-TIME)

These are students who work **full time** for their M. Tech. degree and receive assistantship from the Institute or any other recognized funding agency.

II) SPONSORED (FULL-TIME) STUDENTS

A candidate in the category is sponsored by a recognized R&D organization, national institute, governmental organization or industry for doing M.Tech in the Institute **on a full time basis**. He/she should have at least two years of working experience in the respective field. He/She will not receive any financial support from the Institute. Sponsorship letter (Form I) should be attached with the application. During the course of programme if a regular student secures a job and wishes to join the same, then he/she will be treated as a sponsored candidate and he/she will have to get the sponsorship letter from him employer. He/she would be charged institutional fees as for sponsored candidates.

III) PROJECT STAFF

This category refers to candidates who are working on sponsored projects in the Institute and admitted to the M. Tech. program. The duration of the project at the time of admission should be at least 2 years. This category of students may be registered on a full-time or a part-time basis.

IV) INSTITUTE FACULTY

This category refers to the candidates who are the staff of College of Engineering , Pune, who can attend classes at the Institute while employed. These candidates should be able to attend regular

classes as per the schedule of the Institute. The applicant must be a regular employee of the institute with at least two years of experience with the institute at the time of admission and be engaged in professional work in the discipline in which admission is sought. No financial assistance will be provided by the Institute to such students. A No Objection Certificate from the Head of the Department must be enclosed at the time of applying. This candidate would pay regular fees of the institute under full/part time student category and no concession in institute fees can be allowed.

V) FOREIGN STUDENTS

This category refers to all the Foreign Nationals, who are eligible for Admission to the M.Tech program and who have a certification from the Pune University Foreign Students Cell about their admissions to M.Tech. These students will submit a certificate from the Pune University certifying their Equivalence of Courses at undergraduate levels. These students will have to appear for the institute entrance examination and also a English language test, conducted by the institute. If these students fail in the English language test their applications will be rejected even though they pass in the institute admission test. No financial assistance of any sort will be available for these students. Before admission, these students will have to get a clearance about their background check by the Department of Home, Government of India. A candidate in this category will be admitted **on a full time basis** subject to compliance of various norms laid down by the competent authority from time to time.

3. MINIMUM QUALIFICATIONS

Students for admission to the M. Tech. Program in Engineering Departments must satisfy one of the following criteria:

(i) Bachelor's degree in Engineering/Technology or equivalent in an appropriate area, with a minimum of First Class/60% marks or CGPA of 6.5 on a scale of 10 or equivalent (CGPA of 6.00 or equivalent in case of SC / ST).

(ii) Valid GATE score for Regular (full-time) students.

Departments may specify additional requirements over and above these minimum requirements. All the Non-GATE candidates will have to undergo an entrance test conducted by department in which he/she is applying. Passing in this test will be mandatory for admission.

For the Foreign Students the criteria as in para 2(V) above will be applicable. For these students Institute Admission Test as well as English Test will be mandatory.

4. ADMISSION PROCEDURE

4.1 Admission to the M. Tech. Program of the Institute will normally be in the months of June/July every year. For admission an advertisement will be issued in the month of April/May in National level English news paper, State level Marathi News papers as well as on the Institute website.

4.2 Admission to all the category of students is granted on the basis of GATE scores and / or an interview / admission test held usually during the month of June or July every year. It will be mandatory for every candidate to appear for the Entrance Test and Interview. No absentia of any sort would be allowed.

4.3 The applicants who have completed or are likely to complete all the examinations including the thesis oral examination, viva etc. of the qualifying degree by the date of admission to the program may be considered for admission; however, if admitted, they must produce the evidence of their having passed the qualifying degree examination with the specified minimum marks/CPI (as specified in clause 3) within 8 weeks of the beginning of the semester, failing which their admission is liable to

be cancelled. In case of any dispute or discrepancy decision of the Director COEP and Ex-officio Chairman of the Senate will be final and shall be binding on the candidate.

4.4 Candidates seeking admission for the M.Tech course other than the area in which candidate has completed his/her bachelor's degree will be eligible to apply provided they have a valid GATE score in the area in which they wish to pursue their M.Tech. These candidate will not be eligible for the scholarships from the external funding agencies. These students will have to under go Institute Entrance Test/Interview conducted by the concerned department.

5. FINANCIAL SUPPORT

Students admitted to the M. Tech. Programs will be considered for assistantships, fellowships etc. subject to the following norms:

5.1 A student must have a valid GATE score at the time of admission.

5.2 Students receiving assistantship from the Institute or from any other funding agencies will be required to perform academic duties assigned to them by the departments as per rules in force from time to time.

5.3 The continuation of the assistantship/fellowship will be subject to satisfactory performance of the duties assigned by the department and satisfactory progress in the postgraduate program. Financial assistance of the candidates failing to secure minimum grades in the semester examination would be stopped without any prior notice.

5.4 Financial assistance will normally be for a maximum period of two years. In no case, it will be extended beyond 2 years.

5.5 No financial assistance from the Institute will be available to foreign students. Project staff will get funding from project as per rules but will not get any additional assistance from the Institute.

5.6 Only those students who are currently registered in the postgraduate program shall be entitled to scholarships. The students on leave longer than that specified under the leave rules, and those who are not registered are not entitled to scholarship.

6. LEAVE RULES

6.1 An M Tech student is eligible for maximum 30 days of leave in a calendar year.

6.1.1 The leave of 30 days includes medical and all other leaves, in an academic year. If any Saturday, Sunday or Holiday falls during the leave, they will be counted towards the leave except for such holidays prefixed or suffixed with the leave. **The accumulated leave can be availed during vacation only.**

6.1.2 Out of the 30 days of leave per annum, an M. Tech. Student will be permitted to avail maximum 15 days of leave on completion of each semester. However, any leave not availed at the end of any semester can be carried over to the next semester and the cumulative can be availed together, subject to a maximum of 30 days at a time.

6.1.3 During the semester period, (i.e. July – November and January – May), a student will be allowed only a maximum of 5 days of leave .

6.2 Absence without obtaining prior sanction of leave will be considered as an act of indiscipline and shall entail reduction of scholarship on a prorata basis, besides any other action that may be decided by the Institute.

6.3 Any absence over and above the prescribed limit of admissible leave shall entail deduction from the scholarship, besides other actions as may be decided by the Institute.

6.4 If a student remains absent or discontinues from the course for a period of more than 3 months his/her admission to the course will be automatically cancelled.
6.5 If a student is unable to complete his/her M.Tech within a period of two years, he/she must apply for permission for the extension of time by six months immediately after completion of two years, with recommendations of the concerned guide and head of the department to Dean Academics. Dean academics will seek the approval of the Director COEP and the Chairman, Senate for granting such extensions on case to case basis. Maximum two extensions of six months duration would be permissible for M.Tech student from any category of students as stipulated in Section(2) above. This extension period will not exceed the total period of three years from the date of admission of the candidate in the institute. Candidate will have to pay institute fees prevailing during this extension period.
6.6 If a student fails to complete his/her M.Tech within a period of four years from the date of admission for the course he/she will automatically cease to be a student of the institute and his/her admission would be automatically cancelled.

7. REGULATIONS

7.1 Rules and regulations

All the rules and regulations pertaining to academics, academic calendar, semesters, discipline etc. will be same as that of B.Tech. regulations.

7.2 Admission

Candidates whose selection is approved by the Chairman, Senate will be admitted to the M. Tech. program of the Institute after payment of the prescribed fees prevailing at the time of admission. BOG reserves the right to modify the Institute fees time to time.

7.3 Academic requirements

7.3.1 Semester load and course units

A semester load would be as per the Syllabus structure in force and as recommended/modified by the Senate from time to time. The minimum credit requirements for the successful completion of M.Tech. would be as specified in the syllabus structure prevailing at the time of admission for the course. The current minimum credits for the completion of M. Tech is 80 credits as specified in the syllabus structure. Any changes subsequently made by the Senate in the minimum credit requirements or syllabus structure will be applicable to only the new/fresh students and not applicable to the old candidates.

7.3.2 The residence requirements for students registered in M Tech. is four semesters. They will be required to complete a minimum credits of load as specified in the course structure in force. Every M Tech student must complete prescribed courses as specified in the syllabi structure. SGPA and CGPA will be calculated on the basis of all the courses taken by the student. No regular student/sponsored student/Research Staff/Institute Faculty/ Foreign student registered for the M Tech program shall continue in the program for more than 3 years after the first registration. The course and research requirements in individual departments/program may be over and above the minimum stated here. The departments/program shall obtain prior approval of the Senate of such requirements and will also inform the students in their postgraduate program at the time of their admission.

7.3.3 Grades and points

(a) The performance of the students in their course work will be evaluated in terms of letter grades: AA, AB, BB, BC, CC, CD, DD & F. These grades are equivalent to the following points/ratings on a 10 point scale representing the quality of performance.
AA = 10, AB = 9, BB = 8, BC = 7, CC = 6, CD = 5, DD = 4, FF = 0.
(b) If a student has done a part of the course work, but has for a genuine reason not been able to do the remaining part, the instructor may send the grade 'I' (incomplete). In this case the student must contact the Instructor soon after the examination and if the Instructor is convinced that the reasons for missing a part of the course/examinations are genuine he may let the student make up for the portion missed. The 'I' Grade can be converted into a regular grade by the Instructor within two weeks of the last date of the End Semester Examination. Otherwise, this will automatically be converted into 'F' Grade.

7.3.4. Academic performance requirements

(a) The SGPA (Semester Grade Point Average) or CGPA (Cumulative Grade Point Average) of a student in any particular semester is calculated as follows:
(i) The points equivalent to the grade awarded in each course for which the student has registered is multiplied by its unit rating.
(ii) These products are added and sum is divided by the total number of units. The ratio is the SGPA or CGPA depending on whether the number of units refer to those in that particular semester or to those in the total period of student's postgraduate program.
(b) **The minimum CGPA requirement for continuing in the M. Tech. program is 5.0**. However, M Tech student securing a CGPA between 4.5 and 5.0 may be allowed to continue in the following semester on the recommendation of the DPPC (Departmental Postgraduate Program Committee) and with approval of the Senate.
Students who secure a CGPA below 5.0 in two consecutive semesters will not be allowed to continue in the postgraduate program. Students must obtain a minimum CGPA of 5.0 in order to graduate. In the first semester in which the student registers the minimum CGPA (SGPA) requirement can be relaxed to 4.5.

7.3.5 Thesis/Project

(a) Project duration shall be one year or two semesters. Thesis supervisor(s) for a student will be appointed from amongst the faculty members of the College of Engineering, Pune. Departments will evolve modalities for appointing of supervisors keeping in view the students' aspirations and faculty interest. The DPPC will co-ordinate this activity and will formally communicate the appointment of thesis supervisor(s) of a student to the COE. No change/addition of Supervisor(s) is allowed after the thesis has been submitted to the academic section. In case there has been a change/addition in the Supervisor(s) the thesis will be submitted not earlier than three months from the date of communication of such change/addition to the academic section.

No student once registered for thesis/project units will be allowed to continue the program without a Thesis Supervisor having been appointed by the DPPC. No student will have more than two

supervisors. No change in thesis supervisor(s) will be allowed without the consent of the Chairman, DPPC. In exceptional cases, with prior approval of the Chairman, Senate on the recommendation of the DPPC and COE a student may be allowed to have a co-supervisor from outside the institute.

(b) Project evaluation:

Project evaluation shall be done in two phases in both the semesters. First phase of evaluation shall be in the middle of the semester and second phase of the examination shall be after the end-semester theory examination of the semester.

There will be separate grades awarded for the project course in two semesters. The credits in the first semester shall be relatively less and evaluation shall be based on the literature survey, problem definition, problem formulation, fabrication or software development and preliminary results.

A brief report is required to be submitted at the end of semester. The evaluation and grading will depend on the candidate's performance in the two phases of evaluation in the semester.

The second semester of the project shall carry relatively more weightage and the evaluation shall involve external examiners. The details are provided in the following sub-section.

(c) Thesis/Project Oral Examination Committee :

The thesis/project will be examined by an oral examination committee consisting of the supervisor(s) or in his/her absence the program co-ordinator with prior consent of the supervisor and at least two but not more than four other faculty members of the institute proposed by the thesis supervisor(s)/program co-ordinator in consultation with Head of the Department, recommended by the convener, DPPC and approved by the Dean Academics and COE. The thesis supervisor/program co-ordinator will act as the convener of the committee and one of the members of the committee will be an External Examiner as a part of the panel of examiners.

(d) The Convenor, DPPC will submit to the academic section for approval of the Chairman, DPPC the names of the thesis/project examiners on the prescribed form, at least two weeks before the submission of the thesis. Unbound typed copies of thesis/project one for each examiner prepared according to the prescribed format available in the academic section will be submitted at least one week before the probable date of the oral examination. The oral

examination will be held within two months from the date of submission of the thesis/project. If however the student does not make available for the examination, his/her program will be deemed to have been terminated. Request for revival of the program by such a student should be addressed to the Chairman, Senate.

The Department will record the date of submission of the thesis/project and arrange to send the thesis to the examiners. The supervisor/program co-ordinator will inform the examiners of the date of the oral examination and send a copy to the academic section. The thesis/project will be evaluated and the Oral Examination conducted by the Committee on the scheduled date. The report will be communicated by the Convener, DPPC to the academic section for record and necessary action.

The grade to be awarded to a student shall be evolved by the committee by consensus. The report of the oral examination committee including the grade shall be submitted to the Convenor, DPPC by the committee.

(e) Acceptance/Rejection of the Thesis/Project

A thesis/project will be considered to have been accepted if all members of the committee recommend its acceptance. Otherwise thesis/project will be considered to have been rejected. If a thesis/project is rejected along with a recommendation by the Committee for resubmission after incorporating and modification/correction suggested by the Committee, oral examination for the re-submitted thesis/project will be conducted by the same Committee unless otherwise approved by the Chairman Senate. If the resubmitted thesis/project is rejected, the matter will be reported to the Senate for appropriate action. Acceptance of thesis/project will be reported by the COE to the Senate for approval.

7.3.6. Provision for the Change of Guide

Project Guide may submit his request for change of guide to the HoD of the concerned department stating the reasons for the change request. HOD of the concerned department will forward the Application with his/her recommendations and name of the new proposed guide to the Dean Academics for the permission. Dean Academics in consultation with the Director, COEP and Chairman of the Senate may approve such applications.

Procedure for submission of M. Tech. Project Thesis and Oral Examination

1. The supervisor(s) shall be satisfied that the work has been completed. The supervisor(s) shall forward a list of examiners (comprising of at least two but not more than four faculty members from the department, in addition to the supervisor(s) and one member from outside the department or an external expert) through the Departmental PG Coordinator, to HOD.
2. The HOD will then forward the list of examiners to the Dean of Academics for the approval at least 15 days before submission of the thesis.
3. Following the approval, unbound copies of the thesis (one each for every examiner) shall be submitted to the Department (PG Coordinator) at least one week before probable date of the examination.
4. The PG Coordinator, will fix the date of oral examination, make an announcement (through notices and e-mail) and forward unbound copies of thesis to the examiners. The date of oral examination shall be communicated to the COE.
5. The oral examination of a M. Tech. Project shall be held as per announced schedule and it shall be an open one.
6. The Supervisor / PG Coordinator (if Supervisor is not available at the time of oral examination) shall be the convener of the oral examination committee. The committee shall evaluate the project of the candidate on the basis of presentation of the report, originality of the contents therein, demonstration of equipment model/ hardware/ software developed, the oral presentation and oral examination. In case the committee recommends a major revision and recommends a re-examination of the project, Grade "I" shall be awarded and the student shall be required to continue the project and resubmit the thesis within a period of two months. In case the committee rejects the thesis, Grade "F" shall be awarded and the student shall be required to re-register for the project in the next semester.
7. On successful completion of Oral Examination, each student shall submit bound copies of the thesis making corrections, if any, suggested by the examiners (one each to the supervisor(s), Academic

Section and the department). The academic section will forward the copy of the thesis/report to the Central library after verification.

8. The candidate should also submit a soft copy of the thesis in pdf format to the PG Coordinator who shall compile all the M. Tech project reports of the academic year of the department on a CD and same shall be placed in the dept library and institute website server.

FORM-I

Format of Certificate by the Employer/Management for Sponsored Candidates

This is to certify that ,

Shri./Smt._____

is working in this Institute as _____ since _____and he/she is permitted to study for **M.Tech program** at College of Engineering, Pune. If he/she is admitted to the said program, he/she will be permitted to attend the College as a full time student during the working hours of the College till completion of his/her program. We understand that he/she will fulfill institute norms for the attendance.

This is further to certify that he/she has been appointed on regular basis and his/her appointment is not temporary.

FORM II – APPLICATION FOR THE EXTENSION OF TIME

Reference No.
Date:
To
The Dean Academics,
College of Engineering , Pune

Sub : Grant of six months extension in order to complete M. Tech. Program

Dear Sir,

I of Mr./ Ms .....who is M.Tech student in .....Department and pursuing my M. Tech in .....specialization. I have joined the M.Tech. course in the academic year ..... . I am unable to complete my M.Tech. in the prescribed period of two years. I am aware that maximum duration of my M.Tech. course is four years and my admission for the M.Tech will get cancelled after a period of four years from the date of admission and no extension of time is permissible after three years.

I may be permitted Six months extension for completing M. Tech. Program at your Institute as a full - time student.

Date: Signature of the Student

Recommendation of the Project Guide

FORM III – Undertaking By the Full Time M.Tech (Non-Sponsored Student)

Reference No.
Date:
To
The Dean Academics,
College of Engineering , Pune

Sub : Undertaking by the M.Tech Students who is a Non-Sponsored Full Time Student

Dear Sir,

I of Mr./ Ms ..... is M.Tech student in ……..Department and pursuing my M. Tech in ……..specialization. I have joined the M.Tech course in the academic year …… .

I here by solemnly affirm that I am not in any sort of full time/Part Time or Visiting employment of any sort in any organization while joining my M.Tech as fulltime student. I do here by undertake that I will not engage myself in any sort of employment either fulltime/part time or visiting during my studentship as fulltime M.Tech student of College of Engineering, Pune, unless otherwise I am offered such privilege by COEP under a sponsored project.

I do understand that if I am found to indulge in such employment any time during my tenure as a Full Time M.Tech student of College of Engineering, Pune , my admission to M.Tech course will be immediately cancelled by the institute in addition to financial penalty and other disciplinary action initiated by Dean Academics, on behalf of the institute.

Date: Signature of the Student

Recommendation of the HOD

M Tech (Electronics)

Specialization: VLSI and Embedded Systems

Structure

Semester I

Sr. No.	Course Code	Course Name	Teaching Scheme			Credits
			L	T	P	
1.	OEC I IS-501-16	Image Processing & Analysis	3	--	--	3
2.	PCC I ES-501	PLDs and HDL	3	--	--	3
3.	PCC II ES-503	CMOS VLSI Design	3	--	--	3
4.	PCC III ES-505	Embedded Processors	3	--	--	3
5.	DEC-I ES-513, ES-515	A. Advanced Computer Architecture B. Communication Networks	3	--	--	3
6.	LC ES-509	Course Seminar	--	--	2	1
7.	LLC LL-503	LLC	1	--	--	1
8.	LC ES-511	PG Laboratory I	--	--	6	3
		Total	**16**	**--**	**8**	**20**

Semester II

Sr. No.	Course Code	Course Name	Teaching Scheme			Credits
			L	T	P	
9.	OEC II IS-502-17	Artificial Intelligence and Neural Networks	3	--	--	3
10.	DEC-II ES-510,512	A. High Performance Networks B. Source and Channel Coding Techniques	3	--	--	3
11.	Core IV ES-502	Embedded Software and RTOS	3	--	--	3
12.	PSEC I ES-514,516	A. Memory Technologies B. Reconfigurable Computing	3	--	--	3
13.	PSEC II ES-528,520	A. Advanced Embedded Architecture B. System-on-Chip (SoC)	3	--	--	3
14.	MLC ML-504	Intellectual Property Rights	1	--	--	1
15.	LC ES-508	PG Laboratory II	--	--	8	4
		Total	**16**	**--**	**8**	**20**

Semester-III

Sr. No.	Course Code	Course Name	Teaching Scheme			Credits
			L	T	P	
1	MLC ML-603	Environmental Studies	2	--	--	2
2	MLC ML-601	Constitution of India	2	--	--	2
3	Project ES-601	Project Stage I				16
		Total	4	--	--	20

Semester-IV

Sr. No.	Course Code	Course Name	Teaching Scheme			Credits
			L	T	P	
1	Project ES-602	Project Stage II	--	--	--	20
		Total	--	--	--	20

OEC-I IS-501-16: Image Processing and Analysis

Teaching Scheme
Lectures: 3 hrs/week

Examination Scheme
T1, T2 – 20 marks each, End-Sem Exam – 60

Course outcomes:

At the end of the course, students will demonstrate the ability to:

- Understand the background of image representation and characteristics
- Implement image enhancement, restoration, and image analysis algorithms in both spatial and transform domain
- Study and implementation of image encoding and compression techniques

Syllabus Contents:

Image perception, monochrome and color vision models, Image sampling and quantization, Two dimensional orthogonal transforms - DFT, FFT, WHT, Haar transform, KLT, DCT, Image enhancement, Image restoration Color Image processing, Morphological Image processing, Image Segmentation, Image attribute representation and description Object Recognition

References:

- Gonzalez and Woods, “Digital Image Processing”, Pearson Education.
- Woods and Eddins, “Digital Image Processing using Matlab”, Gonzalez, Pearson Education.
- Milan Sonka, Vaclav Hlavac, Roger Bole, “Image processing , Analysis and Machine Vision”, ITP
- Chanda D. Majumdar, Digital Image Processing and Analysis, PHI
- Pratt W.K, “Digital Image Processing”, John Wiley & Sons

Core-I ES 501: PLDs and HDL

Teaching Scheme
Lectures: 3 hrs/week

Examination Scheme
T1, T2 – 20 marks each, End-Sem Exam - 60

Course outcomes:

At the end of the course, students will demonstrate the ability to:

- Understanding of RTL design and verification techniques and methodologies
- Utilize digital design tools such as Cadence
- Build the local eco-system in VLSI and Semiconductor field.

Syllabus Contents:

Technology scaling, Comparison of Computing Machines. Interconnects, Requirements, Delays in VLSI Structures, Computing Elements, LUT’s, LUT Mapping, ALU and CLB’s,Fine-grained & Coarse-grained structures, Comparison of different architectures viz. PDSPs, RALU, VLIW, Vector Processors, Memories, CPLDs, FPGAs, Partial Reconfigurable Devices, Architectures for existing multi FPGA systems, Modeling combinational and sequential circuits, Design entry by verilog/ VHDL /FSM / SYSTEM C, Hardware modeling with Verilog / VHDL, different verilog /VHDL constructs, and Logic Synthesis, Simulation ,Verification of complex

logic design model

References:

- Charles Roth, Jr, " Digital system design using VHDL", Thomson Asia
- D. J Smith, "HDL chip design: A practical guide for designing synthesizing & simulating ASICs and FPGAs using VHDL and Verilog", Doone publication
- Samir Palnitkar, " Verilog HDL: A guide to digital design& synthesis", Prentice Hall

Core-II ES 503: CMOS VLSI Design

Teaching Scheme
Lectures: 3 hrs/week

Examination Scheme
T1, T2 – 20 marks each, End-Sem Exam - 60

Course Learning Outcomes:

At the end of the course, students will demonstrate the ability to:

- Use mathematical methods and circuit analysis models in analysis of CMOS analog/digital electronics circuits.
- Create models of moderately sized CMOS circuits that realize specified analog/digital functions.
- Apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects..

Syllabus Contents:

MOS Switch, MOS Diode/ Active Resistor, Current Sinks & Sources, High Speed/Frequency Op amps, Technology scaling, Calculations for Area on chip, Power dissipation, PDP, Transmission gate, Domino logic, NORA logic, CMOS layout techniques, Transient response, Advance trends of elements & Alloys for ultra fast logic clock, NMOS, CMOS and Bi CMOS logic gates, W/L and power considerations, subsystem design and layout, ultra fast VLSI circuits and systems with GaAs system. CMOS processing, Threshold voltage adjustment, CMOS analog circuit introduction: Analog integrated circuit design, Analog signal processing, Analog VLSI mix signal design concept, MOS. diode and active resistors, Circuit synthesis and modeling.

References:

- Behzad Razavi, "Design of Analog CMOS integrated circuits".
- Phillip E. Allen and D. Holberg "CMOS Analog Circuit Design", Oxford Publications, 2nd Edition
- Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation"
- Ken Martin "Analog Integrated Circuit Design" , Oxford Press 2000
- Rabey, Chandrakasan, "Digital IC Design", Artech House Publications
- Pucknell and Kamran "Basic VLSI Design" EEE, PHI, 3rd Edition
- Ken Martin, "Digital Integrated Circuit Design"
- ngspice manual for spice coding.

Core-III ES 505: Embedded Processors

Teaching Scheme
Lectures: 3 hrs/week

Examination Scheme
T1, T2 – 20 marks each, End-Sem Exam - 60

Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- Compare and select ARM processor core based SoC with several features/peripherals in view of requirements of embedded applications.
- Install, configure and utilize tool sets for developing applications based on ARM processor core SoC and DSP processor.
- Develop small applications by utilizing the ARM processor core based embedded platform and DSP processor based platform

Syllabus Contents:

The Cortex-M3 processor: Applications, Simplified view – block diagram, programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence, Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations, Code Composer Studio for application development for digital signal processing, On chip peripherals

References:

- Joseph Yiu, “The definitive guide to ARM Cortex-M3”, Elsevier, 2nd Edition
- Venkatramani B. and Bhaskar M. “ Digital Signal Processors: Architecture, Programming and Applications” –Second Edition TMH
- NXP Semiconductor 1768 Microcontroller datasheet and User Manual
- Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publication
- Steve furber, “ARM System-on-Chip Architecture”, Pearson Education
- Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley
- Lapsley P., Bier J., Shoham A., Lee E.A. “ DSP Processor Fundamentals-Architecture and Features” (IEEE Press)
- Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com

DEC-I ES 513: Advanced Computer Architecture

Teaching Scheme
Lectures: 3 hrs/week

Examination Scheme
T1, T2 – 20 marks each, End-Sem Exam - 60

Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- Identify and select the features, hardware and software both, supported by underlying embedded platform.
- Develop and evaluate performance of mini-projects using the above selected embedded platform.
- Incorporate the operating system into the implementation to meet several design constraints.

Syllabus Contents:

Overview of Parallel Processing and Pipelining Processing, Case study of Intel Itanium Processor (IA64), Performance analysis, Principles and implementation of Pipelining, Classification of pipelining processors, advanced pipelining techniques, Software pipelining, VLIW processor, Case study: Superscalar Architecture- Pentium, Ultra SPARC, Vector and Array Processor, FFT Multiprocessor Architecture, Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions, Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Message pass ing parallel programming, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues, Operating systems for multiprocessors systems

References:

- Kai Hwang, Faye A. Briggs, “Computer Architecture and Parallel Processing” McGrawhill international Edition
- Kai Hwang, “Advanced Computer Architecture”, Tata McGrawhill Edition
- V.Rajaraman, L Sivaram Murthy, “Parallel Computers”, PHI.
- William Stallings, “Computer Organization and Architecture, Designing for performance” Prentice Hall, Sixth edition
- Kai Hwang, “Scalable Parallel Computing”, Pearson Education
- Harrold Stone, “High performance computer Architecture”, PHI
- Richard Y. Kain , “Advanced Computer Architecture”, Wiley Publications

DEC-I ES 515: Communication Networks

Teaching Scheme
Lectures: 3 hrs/week

Examination Scheme
T1, T2 – 20 marks each, End-Sem Exam - 60

Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- Understand Protocol rules and algorithms, tradeoffs, rationale
- Deal with Routing, transport, DNS resolution
- Know Network extensions and next generation architecture wireless, mobile, sensors

Syllabus Contents:

Network Design Issues, Network Performance Issues, Networks performance analysis, Protocol Study: Intra and Inter Autonomous system routing protocols, ATM, 802.11, Bluetooth, SNMP, IPV6, Socket Programming, standard application layer Protocols, performance Analysis of the protocols (Mathematical approach), Network Troubleshooting, Network Security, Network Applications, Wireless Networking connecting components & transmission techniques, LAN, WAN, INTRANET, INTERNET, Case studies, and voice over IP, Video conferencing, Digital Library, Network systems design using Network Processors, Study of network processors like Intel's IXP 1200 network processors family.

References:

- Aaron Kershenbaum, "Telecommunication Network Design Algorithms", McGraw Hill, international Editions 1993.
- Vijay Ahuja, "Communications Network Design and Analysis of Computer Communication Networks", McGraw Hill, International Editions.
- Douglas E. Comer, "Internetworking with TCP/IP"
- Douglas E. Comer, "Network Systems Design using Network Processors", Pearson Education

LC ES 511: PG Laboratory - I

Teaching Scheme
Practical: 8 hrs/week

Examination Scheme
Marks - 100

Core II: CMOS VLSI Design Laboratory

Laboratory Outcomes:

At the end of the laboratory work, students will demonstrate the ability to:

- Design of analog CMOS circuits starting from specifications, design and simulation.
- Demonstrate basic analog building blocks and circuit topologies design and characterization.
- Design variables are highlighted and variations in signal swings, bandwidth and gain are characterized.

List of Experiments:

- Introduction to Cadence tool (Simulation and Layout design tool) and basic Red Hat Linux commands, Spartan Kits.
- Design simple Inverter and draw different inverter characteristics.
  - Draw inverter circuit schematic.
  - Transient, DC, and AC analysis of the inverter circuit.

- Design a common source amplifier. Also Draw Schematic and perform transient, DC, AC analysis.
  - By using diode connected load
  - By using current mirror.
- Design a common drain amplifier (Source follower amplifier). Also perform transient, DC and AC analysis.
- Design a differential amplifier with current mirror. Also perform transient, DC and AC analysis.
- Design two stage operational amplifiers Also perform transient, DC and AC analysis

Core III: Embedded Processor Laboratory

Laboratory Outcomes:

At the end of the laboratory work, students will demonstrate the ability to:

- Install, configure and utilize tool sets for developing applications based on ARM processor core SoC and DSP processor.
- Develop a prototype codes using commonly available on and off chip peripherals on the Cortex M3 and DSP development boards

List of Experiments:

Part A)

Experiments to be carried out on Cortex-M3 development boards and using GNU toolchain

- Blink an LED with software delay, delay generated using the SysTick timer.
- System clock real time alteration using the PLL modules.
- Control intensity of an LED using PWM implemented in software and hardware.
- Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
- UART Echo Test.
- Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
- Temperature indication on an RGB LED.
- Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
- Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
- System reset using watchdog timer in case something goes wrong.
- Sample sound using a microphone and display sound levels on LEDs.

Part B)

Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

- To develop an assembly code and C code to compute Euclidian distance between any two points
- To develop assembly code and study the impact of parallel, serial and mixed execution
- To develop assembly and C code for implementation of convolution operation
- To design and implement filters in C to enhance the features of given input sequence/signal

OEC-II IS 502-17: Artificial Intelligence and Neural Networks

Teaching Scheme
Lectures: 3 hrs/week

Examination Scheme
T1, T2 – 20 marks each, End-Sem Exam - 60

Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- Identify and formalize a given problem in the framework of solution by AI methods
- Design Fuzzy Logic based system for engineering applications including AN Network methods
- Deploy inconsistent information systems
- Understanding of major areas and challenges in evolutionary computing and Chaotic systems

Syllabus Contents:

Knowledge Representation: Prepositional Logic, Inference Rules in Prepositional Logic, Knowledge representation using Predicate logic, Predicate Calculus, Semantic net, Frames Inconsistent Information Systems: Basic Concepts of Rough Sets, Equivalence Class and Discernibility Relations, Lower and Upper approximations, Information Systems Framework using Rough Sets, Reducts and Core, Introduction to Rough Set Software ROSE, Rules extractions, Information Gain and applications Evolutionary Computing: Genetic algorithms, Introduction to Genetic Programming Dynamical Systems and Chaos: 1-D Maps, Chaotic orbits, Fixed Points, Chaotic attractors, Bifurcations, Fractals, Mandlebrot set, Time Series analysis Representation and Manipulation of Imprecision and Uncertainty: Type-I Fuzzy Sets, Membership Functions – Triangular, Trapezoidal, PI, T-Norm, S-Norm Operations, Fuzzy Hedges, Fuzzy Relations & Composition, Type-II Fuzzy sets introduction Engineering Adaptations of Fuzzy Systems: Fuzzy Object Class, Fuzzy Logic IC chips, Fuzzy Inference Engine, Rule based fuzzy expert systems, Fuzzy Controllers, case studies Neural Networks: Introduction to neural networks and perception, Neural net Architecture and applications Term Paper: Students in a group will prepare a review term paper on the current topics related to study units in IEEE format and present it in the classes. About 6 papers will be scheduled.

References:

- Toshinori Munakata, “Fundamentals of the New Artificial Intelligence”, Springer, Second Ed
- Elaine Rich, Kevin Knight, B. Nair, “Artificial Intelligence”, Tata Mc Graw-Hill, Third Ed.
- K.T. Alligood, T.D. Sauer, J.A. Yorke, “Chaos-An introduction to Dynamical Systems” Springer
- D. K. Chaturvedi, “Soft Computing- Techniques and its Applications in Electrical Engg.” Springer
- Melanai Mitchell, “An Introduction to Genetic Algorithms (Complex Adaptive Systems)”
- Time Series Analysis Paper by Elizabeth Bradley and Videos by Bradley

DEC-II ES 510: High Performance Networks

Teaching Scheme
Lectures: 3 hrs/week

Examination Scheme
T1, T2 – 20 marks each, End-Sem Exam - 60

Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- Apply knowledge of mathematics, probability, and statistics to model and analyze some networking protocols.
- Design, implement, and analyze simple computer networks.
- Identify, formulate, and solve network engineering problems.
- Knowledge of contemporary issues in computer networks.
- Use techniques, skills, and modern networking tools necessary for engineering practice.

Syllabus Contents:

Types of Networks, Network design issues, Data in support of network design, VoIP system architecture, protocol hierarchy, signaling protocols for VoIP, PSTN gateways, VoIP applications, SCSI, Fiber channel attached storage, Network attached storage including NFS, CIFS and DAFS, Management of network storage architectures, New storage architecture protocols, architectures and enabling technologies, spread spectrum system, system architectures of wireless communication systems, A model for internet security, security attacks, services, internet standards & RFCs, Cryptography, location of encryption devices, key distribution ,Public key cryptography principles and algorithms, RSA algorithm.

References:

- Kershenbaum A., “Telecommunications Network Design Algorithms”, Tata McGraw Hill.
- Ramaswami R., Shivrajan K, “Optical Networks”
- Morgan Kaufmann.,Douskalis B., “IP Telephony: The Integration of Robust VoIP Services”, Pearson Ed. Asia.
- Warland J., Varaiya P., “High-Performance Communication Networks”, Morgan Kaufmann, 1996.
- Stallings W., “High-Speed Networks: TCP/IP and ATM Design Principles”, Prentice Hall, 1998.
- Garg V., Smolk K., Vilkes J., “Applications of CDMA in wireless communication”.
- William Stalling, “Network security, essentials” Pearson education Asia publication.

DEC-II ES 512: Source and Channel Coding Techniques

Teaching Scheme
Lectures: 3 hrs/week

Examination Scheme
T1, T2 – 20 marks each, End-Sem Exam - 60

Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- Appreciate quality/correctness of received information in terms of parameters such as error detection and correction capacity.
- Decide various schemes for encoders and decoders deployability either in software or in hardware forms and its consequences.
- Implement analytical and programming skills on language platforms such as Matlab and 'C' of the students.

Syllabus Contents:

Information and Source Coding for discrete sources, Coding for Discrete Sources-Coding for Discrete Memory-less Sources, Discrete Stationary Sources, Arithmetic coding, transform based lossy coding, JPEG standard and its modes, Color image coding, B/W and color Television standards, Video compression, motion estimation and compensation, MPEG standard-1, 2, 4, Audio coding, psychoacoustic models, ADPCM , MPEG-Audio, Dolby Audio, Channel coding, Channel models, Channel capacity, Linear block codes, Error correction and detection capability, Cyclic codes, Block codes examples such as Hamming codes Convolution codes, Convolution encoding and decoding algorithms such as Viterbi, Sequential and feedback, RS codes and turbo codes

References:

- Bhaskaran, "Image and Video Compression standards and Algorithms", Kluwer Academic press
- Bernard Sklar, "Digital Communication: Fundamentals and Applications", Pearson Education Asia.
- Simon Haykins, "Digital Communication", edition II, Wiley.
- B.P.Lathi, "Modern Digital and Analog Communication Systems", edition III, Oxford press
- Gulati, "Television Engineering", PHI

Core-IV ES 502: Embedded Software and RTOS

Teaching Scheme
Lectures: 3 hrs/week

Examination Scheme
T1, T2 – 20 marks each, End-Sem Exam - 60

Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- Distinguish a real-time system from other systems and evaluate need for real-time operating system

- Implement the real-time operating system principles such as multitasking techniques
- Understand need and structure of implementation of real-time systems.

Syllabus Contents:

RTOS Concepts, Structure of µCOS-II: - Kernel Structure: Tasks, Task States, TCB, Ready List, Task Scheduling, Task Level Context Switching, Locking and unlocking of scheduler, Idle Task, Statistics Task, Interrupts, Clock Tick, Initialization, Starting the OS, Task Management, Time Management, Event Control Blocks, Synchronization in µCOS-II:- Semaphore Management, Mutual Exclusion Semaphores, Event Flag Management, Communication in µCOS-II: - Message Mailbox Management, Message Queue Management, Memory management, MCB, Porting of COS-II: Development Tools, Directories and Files, Configuration and testing of Port, Real Time Application using µCOS-II

References:

- Jean Labrosse, "MicroC/OS-II The Real Time Kernel", CMP Books , 2nd Edition
- David E. Simon, "An Embedded Software Primer", Pearson Education
- Raj Kamal, " Embedded Systems – Architecture: Programming and Design", TMH

PSEC-I ES 514: Memory Technologies

Teaching Scheme
Lectures: 3 hrs/week

Examination Scheme
T1, T2 – 20 marks each, End-Sem Exam - 60

Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- Understand in detail the Designs, Architectures and Applications of semiconductor memory circuits and subsystems.
- Understand the various Fault models, modes and mechanisms in semiconductor memories and their testing procedures.
- Learn state-of-the-art memory chip design.

Syllabus Contents:

Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, SOI, Advanced SRAM Architectures, Application Specific SRAMs; DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM.

Non-Volatile Memories: High Density ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Nonvolatile SRAM, Flash Memories.

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM Fault Modeling, Electrical Testing, Pseudo Random Testing, Megabit DRAM Testing, Nonvolatile Memory Modeling and Testing, IDDQ Fault Modeling and Testing, Application Specific Memory Testing.

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Reliability Modeling and Failure Rate Prediction, Reliability Screening and Qualification. Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging, Future Directions, Introduction to digital tablet PC, LCD, DVD player etc.

References:

- Ashok K. Sharma, "Semiconductor Memories: Technology, Testing and Reliability", Prentice- Hall of India Private Limited, 1997.
- Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience, 2000.
- Wen C. Lin, "Handbook of Digital System Design", CRC Press.
- Kiyoo Itoh, "VLSI memory chip design", Springer International Edition.
- Chenming C Hu, "Modern Semiconductor Devices for Integrated Circuits", Prentice Hall, 1st Ed.

PSEC-I ES 516: Reconfigurable Computing

Teaching Scheme
Lectures: 3 hrs/week

Examination Scheme
T1, T2 – 20 marks each, End-Sem Exam - 60

Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- Understand the basic concepts of Reconfigurable Computing Systems and its usage in developing complete digital systems
- Familiar with several CAD tools used in VLSI design such as Xilinx ISE Foundation,
- Design digital systems for a variety of applications

Syllabus Contents:

Computing requirements, Comparison of Computing Machines, Delays in VLSI Structures, Partitioning and Placement, Routing, Computing Elements, LUT's, LUT Mapping, ALU and CLB's, Fine- grained & Coarse-grained structures, Memories, Arrays for fast computations, CPLDs, FPGAs, Partial Reconfigurable Devices, Hot Reconfiguration; Case study, Architectures for existing multi FPGA systems, Compilation Techniques for mapping applications described in a HDL to reconfigurable hardware, Study of existing reconfigurable computing systems to identify existing system limitations and to highlight opportunities for research, Software challenges in System on chip, Testability challenges; Case studies, Partial reconfigurable design.

References:

- Andre Dehon, “Reconfigurable Architectures for General Purpose Computing”
- Christophe Bobda, “Introduction to Reconfigurable Computing”, Springer Publication.
- Maya Gokhale, Paul Ghaham, “Reconfigurable Computing”, Springer Publication.
- IEEE Journal papers on Reconfigurable Architectures.
- High Performance Computing Architectures (HPCA) Society papers.

PSEC-II ES 528: Advanced Embedded Architecture

Teaching Scheme	Examination Scheme
Lectures: 3 hrs/week	T1, T2 – 20 marks each, End-Sem Exam – 60

Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- Identify and select the features, hardware and software both, supported by underlying embedded platform.
- Understand role and responsibilities of embedded OS
- Develop and evaluate performance of mini-projects using the above selected embedded platform.

Syllabus Contents:

IA32 and IA64 Overview:
Atom processor: Addressing modes: real, big-real, protected, paging, SMM, 64-bit extensions; Registers, Memory accesses and the memory map, Instruction set, Segmentation, Task switching, Paging, Hyper threading, Caches and TLB, Execution pipeline, x86 legacy features, Interrupts, PIC and APIC, Software optimization, VT overview, Front Side Bus (FSB) architecture, Chipset overview, PCI configuration setup, logical PCI bus 0, DDR2, SPD and BIOS, Boot- up sequence, BIOS responsibilities, BIOS configuration, ACPI overview, Power management, Frequency Thermal monitoring, L2 cache power down, Platform power consumption,
Embedded Software Development Suite: Case Studies

References:

- Peter Barry and Patric Crowley, “Modern Embedded Computing”, Morgan Kaufmann
- Lori M. Matassa and Max Domeika, “Break away with Intel Atom Processors – A Guide to Architecture Migration”, Intel Press
- Tom Shanley, “X86 Instruction set Architecture”, Mindshare Press
- Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1:

PSEC-II ES 520: Systems on Chip

Teaching Scheme	Examination Scheme
Lectures: 3 hrs/week	T1, T2 – 20 marks each, End-Sem Exam – 60

Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- Compare CMOS VLSI Technologies along with performance parameters
- Understand design and implementation techniques for data path elements such as ALUs, Multipliers.
- Investigate various power optimization and timing issues related to complex digital systems

Syllabus Contents:

Overview of ASIC types, Hardware/Software co-design issues and its challenges, ASIC design strategies, performance specifications- power, size, speed, Product launch considerations including NRE costs, time to market, flexibility and upgrading the productivity level, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Processor Selection for SoC, Application Specific Instruction Processor (ASIP) concepts.

NISC Control Words methodology, NISC Applications and Advantages, Use of Architecture Description Languages (ADL) for design and verification of Application Specific Instruction-set Processors (ASIP), ADL driven methodologies for design automation of embedded processors, Introduction to EXPRESSION ADL for programmable SoC architectures, No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of GNR (Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors).

Different simulation modes, behavioral , functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, CPLD FPGA architectures, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

Low power SoC design / Digital system, design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis, testing (stuck-at-model, path sensitization, Design for Testability (DFT) and BIST), and verification issues relevant to SoC hardware.

Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs, Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization, Creative applications of SoC in electronic product based systems.

Note: Students will prepare and present a term paper on relevant identified current topics (in batches of three students per topic) as a part of theory course.

References:

- Hubert Kaeslin ETH Zurich, “Digital Integrated Circuit Design: From VLSI Architectures to CMSOS Fabrication”
- B. Al Hashimi, “System on chip-Next generation electronics”
- Rochit Rajsuman, “System-on- a-chip: Design and test”
- P Mishra and N Dutt, “Processor Description Languages”
- *Author Name*, “Processor Design: System-On-Chip Computing for ASICs and FPGAs”
- Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley, 2011

LC ES 508: PG Laboratory - II

Teaching Scheme
Practicals: 8 hrs/week

Examination Scheme
Marks - 100

DEC II: High Performance Networking Laboratory

Laboratory Outcomes:

At the end of the laboratory work, students will demonstrate the ability to:

- Understand design issues and various application areas of High Performance network
- Perform simulations on NS-2 or NS-3 which are free open source simulation platforms.
- Optimize the performance of the networks using different techniques.

List of Experiments:

- Installation and study the features of NS-2.
- Installation and study the features of NS-3.
- Simulate and evaluate the performance of Flow control and Error control protocols for High performance Network.
- Implementation of congestion control protocols for High Performance Networks.
- Implementation of protocols for Quality of Service (QoS) support.
- Performance improvement in Wireless Networks.
- Case study of High Performance Networks.

DEC II: Source Coding and Channel Coding Laboratory

Laboratory Outcomes:

At the end of the laboratory work, students will demonstrate the ability to:

- Acquire skills of C and Matlab programming pertaining to various source and channel coding algorithms
- Understand the principles and intricacies involved in basic data structures and algorithms required for such programming
- Awareness of global data compression standards such as JPEG, MPEG, G.7xx and H.2xx

List of Experiments:

- To design and develop Huffman encoder and decoder in C and Matlab environment
- To design a complete JPEG encoder and decoder with DCT, standard quantization tables, Huffman and Run length encoding
- To design and develop Arithmetic encoder and decoder in C and Matlab environment
- To deploy motion estimation – full search and 2-D logarithmic search algorithms in C and Matlab environment
- To deploy MP3 or AAC based audio/speech encoder and decoder in C and Matlab environment
- To design and develop LBC and Cyclic code – encoder and decoder in C
- For a given constraint length and rate, design and develop a convoultional encoder and decoder(Viterbi or Sequential) in C

Core IV: Embedded Software and RTOS Laboratory

Laboratory Outcomes:

At the end of the laboratory work, students will demonstrate the ability to:

- Understand the features and structures of practical implementations and how application areas impact on real-time operating system facilities.

List of Experiments:

- Controlling of peripherals without using µC/OS -II services.
- Study of Task creation using OSTaskCreate()
- Study of Task creation using OSTaskCreateExt()
- Exploring multitasking features of µC/OS -II.
- Study of Semaphore Service of µC/OS -II.
- Study of Mutex Service of µC/OS -II.
- Exploring Mailbox management Services of µC/OS -II.
- Exploring Message Queue Services of µC/OS -II.
- Study of ISR
- Real Time Application Development using µC/OS –II services.

PSEC - I: Memory Technology Laboratory

Laboratory Outcomes:

At the end of the laboratory work, students will demonstrate the ability to:

- Write synthesizable Verilog code and Verilog test bench for semiconductor memories and target the design to FPGA board.
- Develop skills, techniques and learn state-of-the-art engineering tools (Cadence, Xilinx ISE, Modelsim etc.) to design, implement and test different type of semiconductor memories.
- Design a SRAM, DRAM cell and its associated circuits.

List of Experiments:

- Design a single port ROM & RAM with following specifications:
  - Frequency of operation : 500 MHz
  - Data width : 16 bits
  - Size : 1 MB
- Design a dual port ROM & RAM with following specifications:
  - Frequency of operation : 500 MHz
  - Data width : 16 bits
  - Size : 1 MB
- Design the above configuration with bidirectional port.
- Design DRAM memory of size 1 MB data size 8 bits.
- Design SRAM memory of size 1 MB data size 8 bits.
- Design DDR memory of size 1 MB data size 8 bits.
- Design DDR2 memory of size of 1 MB data size 8 bits.
- Design a 6T SRAM cell using 180nm technology and optimize its Cell ratio and Pull-up ratio.
- Design a Sense amplifier circuit using 6T SRAM and optimize its reading cycles.
- Design a 1T DRAM circuit.

PSEC - I: Reconfigurable Computing Laboratory

Laboratory Outcomes:

At the end of the laboratory work, students will demonstrate the ability to:

- Examine reconfigurable systems for increasing design flexibility
- Learn platform based design methodology to facilitate high degree hardware reuse

List of Experiments:

- To implement migration of various algorithms from software to hardware and study formal verification techniques for reconfigurable SoCs on FPGA interface boards.
- Study practical trade-off among performance, size, power consumption and cost consideration using targeted FPGAs (Performance analysis)
- Study integrated tool/s to enter digital design using block diagram editor and compare with HDL entry

PSEC - II: System on Chip Laboratory

Laboratory Outcomes:

At the end of the laboratory work, students will demonstrate the ability to:

- Study and acquire software skills using modern design tools.
- Obtain adequate knowledge of input, output interfaces

List of Experiments:

The Laboratory sessions will be more as continued experiments to evolve suitable product oriented approaches for end-user applications.

- HDL based design of a simple processor- implementation, testing and verification
- NISC toolkit – installation and experimentation -HDL code synthesis and C based approach for design
- Estimating power consumption of a simple design
- Optimization of area, speed, power parameters for high speed operation
- Study of a ADL environment (select one from LISA, EXPRESSION, GNR)

PSEC - II: Advanced Embedded Architecture Laboratory

Laboratory Outcomes:

At the end of the laboratory work, students will demonstrate the ability to:

- Familiarity with trends and GNU tools used to develop embedded computer system based on embedded OS

List of Experiments:

Hardware Platform: Tunnel Creek boards - A state of art platform based on Intel Atom E6xx processor
Software Platform: Timesys- Fedora 14 OS and GCC tool suite

A. Programming Configurable Registers

- Design MOD 10 counter that accepts pulses and outputs count on seven segment display interfaced using GPIO pins 30-37 provided by I/O chip - Winbond W83627. Use functions inb() and outb() to program the Winbond I/O chip registers to configure the GPIO registers and to control the GPIO pins.
- Design 32 bit adder using 2-bit adder/subtractor as the basic/custom hardware interfaced at GPIO pins 30-37 provided by I/O chip - Winbond W83627. Also, add a new functionality to carry out 32 bit subtraction using the same hardware.
- Write a program to implement calculator to perform multi-digit addition, subtraction, multiplication and division. The calculator program will accept operands and operator from the serial port UARTA of I/O chip - Winbond W83627. The result of the desired operation will be sent via the same serial port. Minicom - terminal emulation utility running on host machine will be forwarding the operands & operator inputted via keyboard and is responsible to display the received result on the screen. Use NULL modem cable to connect the serial ports of Tunnel Creek board and Host machine.

B. Performing all the above experiments given in part ‘A’ using driver APIs.

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MLC - ML504:- Intellectual Property Rights

Teaching Scheme
Lectures : 1 hrs/week

Examination Scheme
T1, T2 – 20 marks each, End-Sem Exam - 60

Course outcomes:

At the end of this course, students will demonstrate the ability.

- Create new ideas, concept to design and generate innovative solutions.
- Write technical patents.
- Apply knowledge for sustainable development

Syllabus Contents:

Introduction: Nature of Intellectual Property: Patents, Designs, Trademarks and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT. Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs. Registered and unregistered trademarks, design, concept, idea patenting.

Reference Books

- Taylor & Francis Ltd, “Resisting Intellectual Property by Halbert”, 2007
- Mayall, “Industrial Design”, Mc Graw Hill
- Niebel, “Product Design”, Mc Graw Hill
- Introduction to Design by Asimov, Prentice Hall
- Robert P. Merges, Peter S. Menell, Mark A. Lemley, “Intellectual Property in New Technological Age”
- T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand.

MLC - ML603: Environmental Studies

Teaching Scheme
Lectures : 1 hrs/week

Examination Scheme
T1, T2 – 20 marks each, End-Sem Exam - 60

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Course Outcomes:

At the end of this course, students will demonstrate the ability to understand

- Importance of environment, its purpose, design and perspectives.

- Analysis of environmental issues related to the exploration of natural resources and development of the mankind.
- Role of professional in protecting the environment for sustainability.
- The solutions for environmental problems created by local, national and global developmental activities.

Syllabus Contents:

Multidisciplinary nature of Environmental studies: Definition, scope and importance, need
Natural Resources: Renewable and non-renewable resources: Natural resources and associated problems. Forest resources: Use and over-exploitation, deforestation, case studies. Timber extraction, mining, dams and their effects on forest and tribal people. Water resources: Use and over-utilization of surface and ground water, floods, drought, conflicts over water, dams-benefits and problems. Mineral resources: Use exploitation, environmental effects of extracting and using mineral resources. Biodiversity and its conservation: Introduction – Definition: genetic, species and ecosystem diversity, Biogeographically classification of India, Value of biodiversity: consumptive use, productive use, social, ethical, aesthetic and option values, Environmental Pollution: Definition, Cause, effects and control measures of Air pollution, Water pollution, Soil pollution, Marine pollution, Noise pollution, Thermal pollution, Nuclear hazards, Solid waste Management. Social Issues and the Environment: From Unsustainable to Sustainable development, Urban problems related to energy, Water conservation, rain water harvesting, watershed management, Resettlement and rehabilitation of people; its problems and concerns.

Reference Books:

- Hazardous Waste Incineration by Brunner R.C.1989, McGraw Hill Inc. 480p
- Marine Pollution by Clark R.S. Clanderson Press Oxford
- Environmental Chemistry by De A.K., Wiley Eastern Ltd.
- Water in Crisis, Pacific Institute for Studies in Dev., Environment & Security by Gleick, H.P. 1993. Stockholm Env. Institute Oxford Univ. Press. 473p
- Global Biodiversity Assessment by Heywood, V.H & Waston, R.T. 1995.. Cambridge Univ. Press
- The Biodiversity of India by Bharucha Erach, Mapin Publishing Pvt. Ltd., Ahmedabad – 380 013,India, Email:mapin@icenet.net
- Handbook of Environmental Laws by Trivedi R.K.,Rules Guidelines, Compliances and Standards,Vol I and II, Enviro Media.

MLC - ML601: Constitution of India

Teaching Scheme
Lectures : 1 hrs/week

Examination Scheme
T1, T2 – 20 marks each, End-Sem Exam - 60

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Course Outcomes:

At the end of this course, students will demonstrate the ability to

- Understand how India has come up with a Constitution which is the combination of the positive aspects of other Constitutions.
- Think laterally to solve problems considering cultural factors of society.

Syllabus Contents:

Preamble to the constitution of India. Fundamental rights under Part – III, details of Exercise of rights, Limitations & Important cases. Relevance of Directive principles of State Policy under Part – IV, Fundamental duties & their significance. Union Executive: President, Prime Minister, Parliament & the Supreme Court of India. State executive: Governors, Chief Minister, State Legislator and High Courts Constitutional Provisions for Scheduled Castes & Tribes, Women & Children & Backward classes. Emergency Provisions. Electoral process, Amendment procedure, 42nd, 44th, 74th, 76th, 86th and 91st Constitutional amendments.

References

- Durga Das Basu, "Introduction to the Constitution of India", Students Edition, Prentice Hall EEE,19th/20th Edn., 2001.
- Charles E.Haries, Michael. S.Pritchard and Michael J.Robins Thompson Asia, "Engineering Ethics", 2003-08-05
- by M.V. Pylee, **"**An Introduction to Constitution of India", Vikas Publishing, 2002.

ES – 601 , ES – 602 : Project Phase I and II

Guidelines for Dissertation Phase – I and II at M. Tech. (Electronics):

- As per the AICTE directives, the dissertation is an year long activity, to be carried out and evaluated in two phases i.e. Phase – I: July to December and Phase – II: January to June.
- The dissertation may be carried out preferably in-house i.e. department's laboratories and centers OR in industry allotted through department's T & P coordinator.
- After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.
- Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.
- **Phase – I deliverables:** A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.
- **Phase – I evaluation:** A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend to repeat the phase-I work.
- During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences OR IP/Patents.
- **Phase – II deliverables:** A dissertation report as per the specified format, developed system in the form of hardware and/or software, A record of continuous progress.
- **Phase – II evaluation:** Guide along with appointed external examiner shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend for extension or repeating the work.

Annexure I

Sample list of Professional Science/Elective courses offered by various departments

Branch Name	Subject Name
Civil Engineering (Construction and Management)	Environmental Impact Assessment
Civil Engineering (Environmental and Water)	Numerical Method
Civil Engineering (Geotechnical Engineering)	Advanced Mathematical Methods
Civil Engineering	Introduction to Coastal Engineering
Civil Engineering	Fortran Programming for Engineering Application
Civil Engineering	Housing and Social aspects of planning
Computer/ Information Technology	Financial Computing
Electrical Engineering (Control System)	Matrix and linear Algebra
Electrical Engineering (Power System)	Wind and Solar Energy
Electrical Engineering (Power System)	Engineering Optimization
Electrical Engineering (Power System)	Linear Systems Theory and Design
Electrical Engineering	Industrial Motion Control
Electronics and Telecommunications (Signal Processing)	Mobile Communication
Electronics and Telecommunications	Applied Statistical Physics
Electronics and Telecommunications(VLSI and Embedded)	Image processing and analysis
Electronics and Telecommunications	Artificial Intelligence
Mechanical Engineering	Finite Element and Boundary Element Methods
Mechanical Engineering	Energy Conservation and Management
Mechanical Engineering	Operation Research
Mechanical Engineering	Introduction to Nuclear Energy
Metallurgical Engineering (Physical/Process)	Electronics and Magnetic Materials
Metallurgical Engineering (Physical/Process)	Thermomechanical Processing of Metals
Metallurgical Engineering	Nanotechnology
Town and Country Planning	Quantitative Techniques
Production Engineering (Manufacturing Engineering and Automation)	Microcontroller and Applications
Production Engineering (Manufacturing Engineering and Automation)	Reliability Engineering
Production	Robot Dynamics and Analysis
Production	Commercial Law
Project Management	Project Planning and Control
Applied Physics	Laser Technology
Mathematics	Complex Analysis
Mathematics	Advanced Mathematical Methods (for all except Mech. and Instru.)
Mathematics	Advanced Mathematics
Mathematics	Engineering Mathematics for Problem Solving
Mathematics	Linear Algebra

Annexure-II:

Sample list of Liberal Learning courses offered at Institute level

Course Outcome:
Student will be able to choose and enhance practical learning and application in the subject of his/her choice.

One credit course spread over the semester to enhance practical learning and application

1. **Agriculture (**Landscaping, Farming, etc.**)**
2. **Business (**Management, Entrepreneurship, etc.**)**
3. **Defense (**Study about functioning of Armed Forces**)**
4. **Education (**Education system, Policies, Importance, etc.**)**
5. **Fine Arts (**Painting, Sculpting, Sketching, etc.**)**
6. **Linguistics**
7. **Medicine and Health (**Diseases, Remedies, Nutrition, Dietetics, etc.**)**
8. **Performing Arts (**Music, Dance, Instruments, Drama, etc.**)**
9. **Philosophy**
10. **Social Sciences (**History, Political Sc., Archeology, Geography, Civics, Economics, etc.**)**