

**M. Tech. (Electronics)**  
**Specialization: Digital Systems**  
**(w. e. f. 2015-16)**  
**Structure**

**List of Abbreviations**

OEC- Institute level Open Elective Course

PSMC – Program Specific Mathematics Course

PCC- Program Core Course

DEC- Department Elective Course

LLC- Liberal Learning (Self learning) Course

MLC- Mandatory Learning Course (Non-credit course)

LC- Laboratory Course

## Semester I

Sr. No.	Course Code	Course Name	Teaching Scheme			Credits
			L	T	P	
1.	OEC	Artificial Intelligence	3	0	0	3
2	PSMC	Mathematics for Digital Systems	3	0	0	3
3.	PCC1	Advanced topics in Computer Architecture	3	0	0	3
4.	PCC 2	Digital design and Verification	3	0	0	3
5.	PCC 3	Image Processing and Computer Vision	3	0	0	3
6.	LC	Advanced topics in Computer Architecture Lab	0	0	2	1
7.	LC	Digital design and Verification Lab	0	0	3	2
8.	LC	Image Processing and Computer Vision Lab	0	0	2	1
9.	LC	Seminar	0	0	2	1
10.	MLC	Research Methodology	1	0	0	0
11.	MLC	Humanities	1	0	0	0
		<b>Total</b>	<b>17</b>	<b>0</b>	<b>9</b>	<b>20</b>

## Semester II

Sr. No.	Course Code	Course Name	Teaching Scheme			Credits
			L	T	P	
1.	PCC 1	DSP Architecture	3	0	0	3
2.	PCC 2	Real Time Operating Systems	3	0	0	3
3.	PCC 3	Digital CMOS VLSI Design	3	0	0	3
4.	DEC 1	(A) Low Power VLSI Design (B) Pattern Recognition and Classification (C) Contemporary Computational Methodologies and Practices	3	0	0	3
5.	DEC 2	(A) High Performance Network (B) Automotive Electronics (C) Crypto-processors	3	0	0	3
6.	LC	DSP Architecture Lab	0	0	2	1
7	LC	Real Time Operating Systems Lab	0	0	2	1
8	LC	Digital CMOS VLSI Design Lab	0	0	2	1
9.	MLC	IPR	1	0	0	1
10.	LLC	Liberal Learning Course	0	0	0	1
		<b>Total</b>	<b>16</b>	<b>0</b>	<b>6</b>	<b>20</b>

**Semester-III**

Sr. No.	Course Code	Course Name	Teaching Scheme			Credits
			L	T	P	
1.	Dissertation	Dissertation Phase - I	--	--	--	14
<b>Total</b>			--	--	--	<b>14</b>

**Semester-IV**

Sr. No.	Course Code	Course Name	Teaching Scheme			Credits
			L	T	P	
1.	Dissertation	Dissertation Phase - II	--	--	--	20
<b>Total</b>			--	--	--	<b>20</b>

## Semester-I

### (OEC) Artificial Intelligence

#### Teaching Scheme

Lectures: 3 hrs/week

#### Examination Scheme

T1, T2 – 20 marks each, End-Sem Exam -60

#### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- CO1: Identify and formalize a given problem in the framework of solution by AI methods
- CO2: Ability to design Fuzzy Logic based system for engineering applications
- CO3: Understanding of major areas and challenges related to Inconsistent Information systems, Evolutionary Computing and Chaotic systems

#### Syllabus Contents:

Knowledge Representation: Propositional Logic, Inference Rules in Propositional Logic, Knowledge representation using Predicate logic, Predicate Calculus, Semantic net, Frames  
Inconsistent Information Systems: Basic Concepts of Rough Sets, Equivalence Class and Discernibility Relations, Lower and Upper approximations, Information Systems Framework using Rough Sets, Reducts and Core, Introduction to Rough Set Software ROSE, Rules extractions, Information Gain and applications  
Evolutionary Computing: Genetic algorithms, Introduction to Genetic Programming  
Dynamical Systems and Chaos: 1-D Maps, Chaotic orbits, Fixed Points, Chaotic attractors, Bifurcations, Fractals, Mandelbrot set, Time Series analysis  
Representation and Manipulation of Imprecision and Uncertainty: Type-I Fuzzy Sets, Membership Functions – Triangular, Trapezoidal, PI, T-Norm, S-Norm Operations, Fuzzy Hedges, Fuzzy Relations & Composition, Type-II Fuzzy sets introduction  
Engineering Adaptations of Fuzzy Systems: Fuzzy Object Class, Fuzzy Logic IC chips, Fuzzy Inference Engine, Rule based fuzzy expert systems, Fuzzy Controllers, case studies  
Neural Networks: Introduction to neural networks and perception, Neural net Architecture and applications  
Term Paper: Students in a group will prepare a review term paper on the current topics related to study units in IEEE format and present it in the classes. About 6 papers will be scheduled.

#### References:

- Toshinori Mankato, “Fundamentals of the New Artificial Intelligence”, Springer, Second Ed
- Elaine Rich, Kevin Knight, B. Nair, “Artificial Intelligence”, Tata Mc Graw-Hill, Third Ed.
- K.T. Alligood, T.D. Sauer, J.A. Yorke, “Chaos-An introduction to Dynamical Systems” Springer.

- D. K. Chaturvedi, “Soft Computing- Techniques and its Applications in Electrical Engg.” Springer.
- Melanai Mitchell, “An Introduction to Genetic Algorithms (Complex Adaptive Systems)” A Bradford Book; Reprint edition ,1998.

### (PSMC)Mathematics for Digital Systems

#### Teaching Scheme

Lectures: 3 hrs/week

#### Examination Scheme

T1, T2 – 20 marks each, End-Sem Exam -60

#### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- CO1: Understands the importance of mathematics and its techniques to solve real life problems.
- CO2: Analyze the applicability of solutions under different system requirements.
- CO3: Study modeling of information sources and different types of coding.

#### Syllabus Contents:

**Transforms:** DFT, DCT and Haar, Properties of DFT, Computation of DFT: FFT and structures, Decimation in time, Decimation in frequency, linear convolution using DFT, Digital filter structures: Basic FIR/IIR filter structures, FIR/IIR Cascaded lattice structures, Parallel all pass realization of IIR.

**Multirate Signal Processing:** Basic structures for sampling rate conversion, Decimators and Interpolators; Polyphase decomposition, Lagrange interpolation, Spline interpolation; polyphase filters, multistage decimator & interpolator, QMF, digital filter banks. Adaptive filters & spectral estimation, Minimum mean square criterion, LMS algorithm, Recursive least square algorithm, DFT in spectral estimation, Applications in subband coding.

**Information and Source Coding for discrete sources:** mathematical models for Information, A Logarithmic Measure of Information: Average and Mutual Information, Entropy, Coding for Discrete Memoryless sources, Discrete Stationary sources, Shannon-Fano and Huffman algorithms, Arithmetic coding, Transform based lossy coding, Channel coding, Channel models, Channel capacity, Linear block codes, Error correction and detection capability, Usefulness of the standard array, Cyclic codes, Block codes examples such as Hamming codes, Convolution codes.

**Cellular Automata:** One dimensional 2 State cellular automata, Wolframs’s Four Classes of CA behavior, CAs as dynamical systems, Langron’s hypothesis, Sznajd model, Two dimensional cellular automata, Significance of CAs for complex systems,

## References:

- M. H. Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley & Sons, Inc., 2002.
- S. Haykin, “Adaptive Filter Theory”, Prentice Hall, 2001.
- D.G. Manolakis, V.K. Ingle and S.M. Kogon, “Statistical and Adaptive Signal Processing”, McGraw Hill, 2000.
- Bhaskaran, “Image and Video Compression standards and Algorithms”, Kluwer Academic press.
- B.P.Lathi, “Modern Digital and analog Communication Systems”, Edition III, Oxford Press.

## (PCC 1) Advanced Topics in Computer Architecture

### Teaching Scheme

Lectures: 3 hrs/week

### Examination Scheme

T1, T2 – 20 marks each, End-Sem Exam -60

### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- CO1: Identify and select the features, hardware and software both, supported by underlying embedded platform.
- CO2: Develop and evaluate performance of mini-projects using the above selected platform.

### Syllabus Contents:

**Parallel Processing and Pipelining Processing-** Architectural Classification, Applications of parallel processing, Instruction level Parallelism and Thread Level Parallelism, Explicitly Parallel Instruction Computing (EPIC) Architecture, Pipeline Architecture-Principles and implementation of Pipelining, Classification of pipelining processors, Design aspect of Arithmetic and Instruction pipelining, Pipelining hazards and resolving techniques, Data buffering techniques, Advanced pipelining techniques, Software pipelining, VLIW (Very Long Instruction Word) processor.

**Vector and Array Processor-** Issues in Vector Processing, Vector performance modeling, SIMD Computer Organization, Static Vs Dynamic network, Parallel Algorithms for Array Processors: Matrix Multiplication.

**Multiprocessor Architecture** - Loosely and Tightly coupled multiprocessors, Inter Processor communication network, Time shared bus, Multiport Memory Model, Memory contention and arbitration techniques, Cache coherency and bus snooping, Massively Parallel Processors (MPP).

**Multithreaded Architecture-** Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions, Parallel Programming Techniques: Message passing program development.

**Parallel algorithms for multiprocessors-** Classification and performance of parallel algorithms, Operating systems for multiprocessors systems, Message passing libraries for parallel programming interface, PVM (in distributed memory system), Message Passing Interfaces (MPI). MIPS on FPGA

**References:**

- Kai Hwang, Faye A. Briggs, “Computer Architecture and Parallel Processing” Mc-Graw Hill, International Edition.
- Kai Hwang, “Advanced Computer Architecture”, McGraw-Hill, 1993.
- William Stallings, “Computer Organization and Architecture, Designing for performance” Prentice Hall, Sixth edition.
- Kai Hwang, “Scalable Parallel Computing”. McGraw-Hill, 1998.
- Harold S. Stone “High-Performance Computer Architecture”. Addison-Wesley, 1993.

**(PCC 2) Digital design and Verification**

**Teaching Scheme**

Lectures: 3 hrs/week

**Examination Scheme**

T1, T2 – 20 marks each, End-Sem Exam -60

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

- CO1: Understanding of RTL design and verification techniques and methodologies.
- CO2: Have job opportunities in semiconductor industry or in academics.
- CO3: Build the local eco-system in VLSI and Semiconductor field.

**Syllabus Contents:**

Revision of basic Digital systems: Combinational Circuits, Sequential Circuits, Logic families. Synchronous FSM and asynchronous design, Metastability, Clock distribution and issues, basic building blocks like PWM module, pre-fetch unit, programmable counter, FIFO, Booth's multiplier, ALU, Barrel shifter etc.

Verilog/VHDL Comparisons and Guidelines, Verilog: HDL fundamentals, simulation, and test-bench design, Examples of Verilog codes for combinational and sequential logic, Verilog AMS

System Verilog and Verification: Verification guidelines, Data types, procedural statements and routines, connecting the test bench and design, Assertions, Basic OOP concepts, Randomization, Introduction to basic scripting language: Perl, Tcl/Tk

Current challenges in physical design: Roots of challenges, Delays: Wire load models Generic PD flow, Challenges in PD flow at different steps, SI Challenge - Noise & Crosstalk, IR Drop, Process effects: Process Antenna Effect & Electromigration

Programmable Logic Devices: Introduction, Evolution: PROM, PLA, PAL, Architecture of PAL's, Applications, Programming PLD's, FPGA with technology: Antifuse, SRAM, EPROM, MUX, FPGA structures, and ASIC Design Flows, Programmable Interconnections, Coarse grained reconfigurable devices

IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, and Use of external hard IP during prototyping, Case studies, and Speed issues.

Testing of logic circuits: Fault models, BIST, JTAG interface

### References:

- Douglas Smith, "HDL Chip Design: A Practical Guide for Designing, Synthesizing & Simulating ASICs & FPGAs Using VHDL or Verilog", Doone publications 1998.
- Samir Palnitkar, "Verilog HDL, A guide to Digital Design and Synthesis", Prentice Hall.
- Doug Amos, Austin Lesea, Rene Richter, "FPGA based Prototyping Methodology Manual", Synopsys Press.
- Christophe Bobda, "Introduction to Reconfigurable Computing, Architectures, Algorithms", Springer Netherlands.
- Janick Bergeron, "Writing Testbenches: Functional Verification of HDL Model", Second Edition, Springer 2003.

## (PCC 3) Image Processing and Computer Vision

### Teaching Scheme

Lectures: 3 hrs/week

### Examination Scheme

T1, T2 – 20 marks each, End-Sem Exam -60

### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- CO1: Understand the background of image representation and characteristics.
- CO2: Implement image enhancement, restoration, and image analysis algorithms in both spatial and transform domain and write algorithms of image analysis in transform domain.
- CO3: Study and implementation of image encoding, compression techniques and motion estimation techniques.

### Syllabus Contents:

Concepts and techniques for image processing and computer vision; representation and process image/video signals; image acquisition and display using digital devices, properties of human

visual perception, sampling and quantization , image enhancement, image restoration, 2-D Fourier transform, linear and non linear filter, morphological operations, noise removal, image deblurring, edge detection, image registration and geometric transformation, segmentations, image reconstruction, image and video compression, Motion estimation: Differential motion analysis methods, optical flow, detection of specific motion patterns, image stitching, motion models for tracking, alignments, compositing.

**References:**

- Anil K. Jain “Fundamentals of Digital image processing”, PHI, 2010.
- Rafael C. Gonzalez and Richard E. Woods, “Digital Image Processing”, Pearson, Third Edition, 2008.
- Shilpa Metkar, Sanjay Talbar, “Motion Estimation Techniques for Digital Video Coding”, Springer 2013.
- M. A. Joshi, “Digital Image Processing: An Algorithm Approach”, PHI, 2006
- Shapiro and Stockman, “Computer Vision”, Prentice Hall, 2001.
- Forsyth, David A., Ponce, Jean, “Computer Vision: A Modern Approach” 2nd Edition Pearson, 2012.

**Lab for Semester –I**

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

- Apply the knowledge under supervision to solve engineering problems in the core field.
- Use the techniques, skills and modern engineering tools necessary for engineering practices.
- Identify and code the module using different modeling styles.

Simulation & Programming on System Modeling using programming environments (C-Compiler / MATLAB/ other Simulation Tools)

Design and Implementation of Combinational and Sequential Circuits using Simulation Tools as ISE Design Suite/Vivado design suite(Xilinx) / ngspice(open source)/ QuestaSim (Mentor Graphics). Experimenting on Xilinx /Altera CPLD/FPGA.

**Students will solve four assignments based on each core course.**

## (LC) Advanced Computer Architecture Lab

### Teaching Scheme

Practical: 2 hrs/week

### Examination Scheme

Term work/Practical: 100 Marks

### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

CO: The assignments will give in site understanding of new micro-architectures based on various parameters of the instructions used by processors.

### List of assignments:

- 1) Convert a c code into assembly code for particular processor with the help of processors data sheet.
- 2) Write C program for branch prediction. History table has to be created in the program to help for prediction. Find the possibility of instruction rescheduling in the program and calculating the branch penalty possibilities.
- 3) Write C program to find data dependencies of a given .asm file for a pipelined processor.
- 4) Write C program to find control dependencies of a given .asm file for a pipelined processor.
- 5) Draw data path for MIPS instruction set (any three).
- 6) Control the pipeline by scoreboarding technique for multiple issue / multiple output situation.
- 7) Array processing using p-thread library to exploit parallel processing on dual core processor. Analyze the performance of parallel processing in terms of processing time.
- 8) Finding the cache miss and cache hit from given example of program.

## (LC) Digital design and verification Lab

### Teaching Scheme

Practical: 2 hrs/week

### Examination Scheme

Term work/Practical: 100 Marks

### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- Understand the programmable and reprogrammable systems
- Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.
- Simulate the design with test benches and synthesizing & implementing these designs

with FPGA development boards including interfacing to external devices with the help of EDA tools like Cadence, Mentor Graphics and Xilinx.

### List of assignments:

- Designing combinational logic using MSI devices:

Octal tristate buffer MUX/DeMUX , ALU, Priority encoder, Booths Multiplier

- Designing sequential logic:

Up/down counter, Barrel shifter, Memory model, Shift register, Bus arbitration logic, State machine/vending machine, RISC CPU

PCI Bus and Arbiter UART / USART implementation Realization of single port SRAM

Discrete Fourier transform or Fast Fourier Transform algorithm in verilog.

Lab Journal: In the form of CD (Should contain Coding, snapshot of result, synthesis report, RTL view, pre & post synthesis and implementation reports)

### (LC) Image Processing and Computer Vision Lab

#### Teaching Scheme

Practical: 2 hrs/week

#### Examination Scheme

Term work/Practical: 100 Marks

#### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- CO1: Denoise of images, Linear filtering of images
- CO2: Apply the principles of segmentation, grouping and modeling in image processing and computer vision.
- CO3: use the principles of motion and tracking in image sequences (video)

#### Laboratory assignments:

1. Image Manipulation: Read, write, view images and conversion between different formats.
2. Spatial Transformations: Convolution and correlation
3. Frequency Transformations: Fourier transform, explore histogram as an enhancement technique.  
.Filtering, Noise identification and removing the same using filtering techniques
5. Morphological Transformations: Dilatation and erosion as fundamental morphological operations.

6. Segmentation using Edge Detection: Detection of boundaries between two regions using different gradient approximations.
7. Segmentation using Thresholding: Divide the image in regions depending on the gray level.
8. DCT based image compression
9. Image stitching
10. Object tracking

### (LC) Seminar

#### Teaching Scheme

Practical: 2 hrs/week

#### Examination Scheme

Marks: 100

#### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- CO1: Identify, understand and discuss current, real-world issues.
- CO2: Improve oral and written communication skills.
- CO3: Apply principles of ethics and respect in interaction with others.

#### Guidelines:

- **Selection of Topic:**
  - Select a topic relevant to the stream of study with content suitable for M. Tech. level presentation. For selection topics refer internationally reputed journals. The primary reference should be published during the last two or three years.
  - Some of the journals/publications suitable for reference are: IEEE/the IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication - Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain
  - Get the topic approved by the seminar guide well in advance.
- **Preparation of Presentation and Report:**
  - In slides, list out key point only. You may include figures, charts equations tables etc. but not running paragraphs. Font size used should be at least 20.
  - Figures should be very clear and possibly drawn by you using suitable software tools. There should be a slide on “Conclusion”.

- A report of the seminar should be prepared which should contain the following.
  - o Title of the seminar.
  - o Name and other details of presenter and the guide.
  - o Abstract of the topic.
  - o Contents such as Introduction, Theory to elaborate the concept, Implementation if carried out by the presenter/or fellow researcher/s, Comparison with other relevant techniques, Conclusion etc.
  - o List of references strictly in IEEE format.
- **Oral Presentation:**
  - Student needs to orally present the topic for 20 minutes with good voice projection and with modest pace
- **Answering Queries:**
  - Student needs to answer queries raised by the audience and evaluators. This session shall be restricted to 5 minutes. In case of more queries, student is supposed to solve the queries offline.

### (MLC) Research Methodology

#### Teaching Scheme

Lectures: 1 hrs/week

#### Examination Scheme

End-Sem Exam - 50

#### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- CO1: Understand research problem formulation.
- CO2: Analyze research related information
- CO3: Follow research ethics

#### Syllabus Contents:

- Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem.
- Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

- Effective literature studies approaches, analysis
- Plagiarism , Research ethics,
- Effective technical writing, how to write report, Paper
- Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

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### References:

1. Stuart Melville and Wayne Goddard, “Research methodology: an introduction for science & engineering students”
2. Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”
3. by Ranjit Kumar, 2 nd Edition , “Research Methodology: A Step by Step Guide for beginners”

### (MLC) Humanities

#### Teaching Scheme

Lectures: 1 hrs/week

#### Examination Scheme

Mid sem-20, Assignment/quiz-50

End Sem Exam- 30

#### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- CO1: Understand the need, basic guidelines, content and process for value education.
- CO2: Understand the harmony in the family, difference between respect and differentiation
- CO3: Understand the harmony in nature, interconnectedness and mutual fulfillment in nature, holistic perception of harmony.
- CO4: Understand natural acceptance of human values, competence in professional ethics.

## **Syllabus contents:**

### **Unit 1 Communication skills**

Introduction to the scope and significance of learning Humanities. And communication.

- Comprehension
- Written communication: Formal letters, CV, Reports, Paragraphs
- Grammar and Vocabulary building exercises

### **Unit 2**

#### **Social Science and Development**

Indian and western concept, Process of social change in modern India, Impact of development of Science and technology on culture and civilization, Urban sociology and Industrial sociology  
Social problems in India: overpopulated cities, no skilled farmers, unemployment, addictions and abuses, illiteracy, too much cash flow, stressful working schedules, nuclear families etc.

### **Unit 3**

#### **Technology assessment and transfer**

Sociological problems of economic development and social change

Assessment and transfer of technology, problems related with tech transfer with reference to India, Roles of an engineer in value formation and their effects on society

#### **References:**

1 English for everyone – Mcmillan (India) Ltd.

2 Jude paramjit S and Sharma Satish K, “Ed: dimensions of social change”

3 Raman Sharma, “Social Changes in India”

## Semester- II

(PCC 1)      DSP Architecture

### Teaching Scheme

Lectures: 3 hrs/week

### Examination Scheme

T1, T2 – 20 marks each, End-Sem Exam -60

### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- CO1: Identify and formalize architectural level characterization of Programmable -DSP hardware.
- CO2: Design, programming (assembly and C), and testing code using Code Composer Studio for single core and multi core DSP systems.
- CO3: Deployment of DSP hardware for Control, Audio and Video Signal processing applications.

### Syllabus Contents:

**Programmable DSP Hardware:** Processing Architectures (von Neumann, Harvard), DSP core algorithms (FIR, IIR, Convolution, Correlation, FFT), IEEE standard for Fixed and Floating Point Computations, Special Architectures Modules used in Digital Signal Processors (like MAC unit, Barrel shifters), On-Chip peripherals, DSP benchmarking.

**Structural and Architectural Considerations:** Parallelism in DSP processing, Texas Instruments TMS320 Digital Signal Processor Families, Fixed Point TI DSP Processors: TMS320C1X and TMS320C2X Family, TMS320C25 –Internal Architecture, Arithmetic and Logic Unit, Auxiliary Registers, Addressing Modes (Immediate, Direct, and Indirect, Bit-reverse Addressing), Basics of TMS320C54x and C55x Families in respect of Architecture improvements and new applications fields, TMS320C5416 DSP Architecture, Memory Map, Interrupt System, Peripheral Devices, Illustrative Examples for assembly coding.

**VLIW Architecture:** Current DSP Architectures, GPUs as an alternative to DSP Processors, TMS320C6X Family, Addressing Modes, Replacement of MAC unit by ILP, Detailed study of ISA, Assembly Language Programming, Code Composer Studio, Mixed C and Assembly Language programming, on-chip peripherals, Simple applications developments as an embedded environment.

**Multi-core DSPs:** Introduction to Multi-core computing and applicability for DSP hardware, Concept of threads, introduction to P-thread, mutex and similar concepts, heterogeneous and homogenous multi-core systems, Shared Memory parallel programming - OpenMP approach of parallel programming, PRAGMA directives, OpenMP Constructs for work sharing like for loop, sections, TI TMS320C6678 (Eight Core subsystem).

**High Performance Computing using P-DSP:** Preliminaries of HPC, MPI, OpenMP, multicore DSP as HPC infrastructure.

- Lapsley P., Bier J., Shoham A., Lee E.A. - DSP Processor Fundamentals-Architecture and Features (IEEE Press).
- TI User Manuals TMS320C2x, TMS320C5x, TMS320C54x, TMS320C62x, TMS320C6713 Website [www.ti.com](http://www.ti.com) and, [www.DSPguide.com](http://www.DSPguide.com)
- Smith, S. W., “The Scientist and Engineer's Guide to Digital Signal Processing”, California Technical Publisher, 1998.
- Craig Marven, Gillian Ewers , “A simple approach to DSP” , Wiley-Blackwell, 1996.
- Kuo S.M. and Lee B. H , “Real Time Digital Signal Processing Implementation Applications and Experiments with TMS 320C55X” John Willey and Sons 2001.

## (PCC 2) Real Time Operating Systems

### Teaching Scheme

Lectures: 3 hrs/week

### Examination Scheme

T1, T2 – 20 marks each, End-Sem Exam -60

### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- CO1: Distinguish a real-time system from other systems and evaluate need for real-time operating system.
- CO2: Implement the real-time operating system principles such as multitasking techniques.
- CO3: Understand need and structure of implementation of real-time systems.

### Syllabus Contents:

**RTOS Concepts:** Foreground and background systems, Critical section, Shared Resources, Tasks, Multitasking, Context Switching, Kernels, Pre-emptive and non pre-emptive Schedulers, Static and Dynamic Priorities, Priority Inversion, Mutual exclusion, Synchronization, Inter task Communication mechanisms, Interrupts: Latency, Response and recovery, Clock Tick, Memory Requirements.

**Structure of  $\mu$ COS-III** - Kernel Structure: Tasks, Internal Tasks, Task States, TCB, Ready List, Task Scheduling, Task Level Context Switching, Locking and unlocking of scheduler, , Interrupt Management, Direct and Deferred Post Methods, Initialization, Starting the OS, Task Management, Time Management, Timer Management, Event Control Blocks, Synchronization in  $\mu$ COS-III - Semaphore Management, Mutual Exclusion Semaphores, Event Flag Management, Communication in  $\mu$ COS-III - Message Queue Management, Memory management, MCB, Porting of  $\mu$ COS-III: Development Tools, Directories and Files, Configuration and testing of Port, Real Time Application using  $\mu$ COS-III. Directories and Files.

**References :**

- Jean Labrosse, “ MicroC/OS-II The Real Time Kernel”, CMP Books , 2nd Edition.
- “ $\mu$ C/OS-III: The Real-Time Kernel for the Texas Instruments Stellaris MCUs”
- David E. Simon, “An Embedded Software Primer”, Addison-Wesley Professional, 1999.
- Raj Kamal, “Embedded Systems – Architecture: Programming and Design”, Tata McGraw-Hill Education, 2003.

**(PCC 3) Digital CMOS VLSI Design****Teaching Scheme**

Lectures: 3 hrs/week

**Examination Scheme**

T1, T2 – 20 marks each, End-Sem Exam -60

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

- CO1: Analyze, design, optimize and simulate simple and complex digital circuits using CMOS according to the design metrics.
- CO2: Connect the individual gates to form the building blocks of a system.
- CO3: Use EDA tools like Cadence, Mentor Graphics and other open source software tools

**Syllabus Contents:**

**MOS Transistor Theory:** Physical structure of MOS transistor, MOS transistor under static conditions, secondary effects, SPICE models for MOS transistor, Process variation, Technology Scaling

**The Manufacturing Process:** Manufacturing CMOS integrated circuits, design rules, packaging integrated circuits, trends in process technology

**CMOS Inverter:** CMOS inverter, Static and Dynamic behavior of CMOS inverter, Power, Energy and Energy-Delay, Technology Scaling and Impact on inverter Metrics

**Combinational Logic Designs in CMOS:** Static CMOS design, Dynamic CMOS Design, Examples

**Sequential Logic Designs in CMOS:** Introduction, Static latches and registers, Dynamic latches and registers, Pipelining, Examples

**Designing Arithmetic Building Blocks:** Adders, Multipliers, Shifters, Power and Speed Trade-Off in Data path Structures

**References:**

- Jan Rabaey, Anantha C , Borivoje Nikolic “Digital integrated circuits- A design perspective”, 2nd edition, PHI.
- Kamran Eshraghian, Pucknell and Eshraghian, “Essentials of VLSI Circuits and Systems”, Prentice-Hall (India).
- Kang, Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, TATA McGRAW Hill.
- Wayne Wolf, “Modern VLSI Design”, Pearson Education.
- Neil Wieste, David Harris, Ayan Banerjee, “CMOS VLSI Design”, ,3rd Edition, Pearson Education , 2008.

**(DEC-I) (A) Low Power VLSI Design****Teaching Scheme**

Lectures: 3 hrs/week

**Examination Scheme**

T1, T2 – 20 marks each, End-Sem Exam -60

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

- CO1: Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
- CO2: Characterize and model power consumption & understand the basic analysis methods.
- CO3: Understand leakage sources and reduction techniques.

**Syllabus Contents:**

**Technology & Circuit Design Levels:** Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of  $V_{dd}$  &  $V_t$  on speed, constraints on  $V_t$  reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations

**Low Power Circuit Techniques:** Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches

**Low Power Clock Distribution:** Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. tolerable skew, chip & package co-design of clock network.

**Logic Synthesis for Low Power estimation techniques:** Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers

**Low Power Memory Design:** Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits

**Low Power Microprocessor Design System:** power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

### References:

- P. Rashinkar, Paterson and L. Singh, “Low Power Design Methodologies”, Kluwer Academic, 2002
- Kaushik Roy, Sharat Prasad, “Low power CMOS VLSI circuit design”, John Wiley sons Inc.,2000
- J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley, 1999.
- A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995
- Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.

### (DEC-I) (B) Pattern Recognition and Classification

#### Teaching Scheme

Lectures: 3 hrs/week

#### Examination Scheme

T1, T2 – 20 marks each, End-Sem Exam -60

#### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- CO1: Understand object description, recognition techniques, design and implement classification techniques,
- CO2: Understand the mathematical concepts of pattern recognition.
- CO2: Apply AI techniques to object detection and classification.

#### Syllabus Contents:

Shape representation and description : Region identification, contour based shape representation and description, chain codes, simple geometric border representation, Fourier transforms of boundaries, boundary description using segment sequences, B spline representation, other contour based shape description approaches, Shape invariants, Region based shape representation and description, Simple scalar region descriptors, moments, convex hull, graph based on region skeleton, region decomposition, region neighborhood graphs, shape classes.

Mathematical morphology: Basic morphological concepts, morphological principles, binary dilation and erosion, hit or miss transformation, opening and closing, gray scale dilation and erosion, thinning and skeletonization, gray scale dilation and erosion properties of erosion and dilation, opening and closing, top hat transformation, statistical texture description, methods based on spatial frequencies, co-occurrence matrices, edge frequency, other statistical methods of texture description.

Knowledge representation and decision making, Knowledge representation, statistical pattern recognition, classification principles, classifier setting, classifier learning, Baye"s classification, nearest neighbor classification, cluster analysis. Artificial neural networks and fuzzy systems: Neural nets, feed forward networks, unsupervised learning, Hopfield neural nets, optimization techniques in recognition, genetic algorithms, simulated annealing, fuzzy systems, fuzzy sets and fuzzy membership functions, fuzzy set operators, fuzzy reasoning, fuzzy system design and training, Back propagation algorithm

**References:**

- Richard Duda, Peter Hart, David Stork, "Pattern Classification", Second Edition John Wiley and Sons Inc., 2005
- Rajjan Shinghal, "Pattern Recognition: Techniques and Applications", Oxford University Press, 2006
- Milan Sonka, Vaclav Hlavac, Roger Boyle, "Image Processing, Analysis, and Machine Vision" Brooks/Cole; 3rd edition (1 March 2007)
- Madhuri A. Joshi, Mehul S. Raval, Yogesh H. Dandawate, Kalyani R. Joshi, Shilpa P. Metkar "Image and Video Compression: Fundamentals, Techniques, and Applications" CRC Press.

**(DEC-I) (C) Contemporary Computational Methodologies and Practices**

**Teaching Scheme**

Lectures: 3 hrs/week

**Examination Scheme**

T1, T2 – 20 marks each, End-Sem Exam -60

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

- CO1: Learn to analyze algorithms and estimate performance behavior (time and space) and practice the object-oriented programming style for applications in signal processing, embedded system algorithms, genetic algorithms. (C++ and /or Java depending on requirements of R&D grants/projects in the department).
- CO2: Apply simulation techniques to formulate performance evaluation for Communication and computer systems.
- CO3: Assess impact of algorithms, coding practices, on performance of reliable embedded systems for critical applications (non-consumer electronics sector).

## **Syllabus Contents:**

### **Performance Evaluation of Computer System and Communications systems**

Performance Evaluation of – workload characterization and techniques, Capacity Planning, Experimental design Monte Carlo simulation, Probability distributions, Random variates, Queueing theory, ARENA simulation software

### **Fault-tolerant Embedded System:**

Introduction to system reliability and embedded systems, Component failure rate, Embedded software disasters, Software failure mechanism, Software reliability metrics, Software fault tolerance and recovery block scheme in embedded systems, Minimizing code size and real time requirements, Estimating fault content using analysis of complexity and Regressing Tree Modeling, SFMEA, SFTA, Software reliability tools-CASER, SRTPro, SREPT

### **Design and Analysis of Algorithms:**

Iterative Algorithms design issues- Complexity calculations, Big O, Theta, Omega notation, Computational models and design by refinements- Functional and Imperative models , design using recursion, Abstract algorithms- Divide and Conquer, Timing analysis, Greedy methods, Dynamic Programming, Backtracking , Algorithm analysis- Complexity Calculations for sorting algorithms, Time Space Tradeoffs, Randomized algorithms, Genetic algorithms introduction, NP-Hard and NP-complete Problems- Basic concepts, Cook's theorem, NP-Hard Graph Problems, NP - Hard Scheduling Problems. NP -Hard Code Generation

### **Digital Forensic, Cyber Security, IT Act 2000**

Computer Forensic Hardware, Disc capacity and transfer rate measurement conventions, Forensic Write Blockers, Recovering Image files, Network forensic, Computer forensic analysis device -Shadow 3, introduction to Tableau TD2 kit (forensic duplicator), Encase7, Reverse engineering Information security view from critical infrastructure perspective, Impact of Electronic and computing hardware infrastructure on e-Governance, BPO, and smart city projects vis-à-vis provisions of Information Technology Act 2000, Introduction to Semiconductor Integrated Circuits Layout Design Act (SICLD), 2000

### **Object Oriented Programming Systems:**

Object oriented Programming- C-basic data types, user defined data types, structures and functions, C++ Classes and Objects, C++ constructors and destructors, inheritance, overloading and information hiding, namespace scope, Object oriented mechanisms in Java, Exception handling, threads and multithreads

### **References:**

1. R. Jain, "The Art of Computer Systems Performance Analysis: Techniques for Experimental Design, Measurement, Simulation, and Modeling," Wiley- Interscience
2. D.C. Montogormy, " Design and analysis of experiments" , Wiley

3. PH Dave, HB Dave, “Design and Analysis of Algorithm”, Pearson Education
4. R. Pannerselvam, “ Design and Analysis of Algorithms”, University Science Press,
5. Bill Nelson, Amelia Phillips, Christopher Steuart, “Guide to Computer Forensics & Investigation”, Cengage Learning,

### **(DEC-II) (A) High Performance Networks**

#### **Teaching Scheme**

Lectures: 3 hrs/week

#### **Examination Scheme**

T1, T2 – 20 marks each, End-Sem Exam -60

#### **Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

- CO1: Apply knowledge of mathematics, probability, and statistics to model and analyze some networking protocols and apply Knowledge of contemporary issues in computer networks.
- CO2: Use techniques, skills, and modern networking tools necessary for engineering practice.
- CO3: Evaluate performance of Networks.

#### **Syllabus Contents:**

**Types of Networks**, Network design issues, Data in support of network design. Network design tools, protocols and architecture. Streaming stored Audio and Video , Best effort service, protocols for real time interactive applications, Beyond best effort, scheduling and policing mechanism, integrated services, RSVP-differentiated services.

VoIP system architecture, protocol hierarchy, Structure of a voice endpoint, Protocols for the transport of voice media over IP networks. Providing IP quality of service for voice, signaling protocols for VoIP, PSTN gateways, VoIP applications

VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN. MPLS-operation, Routing, Tunneling and use of FEC, Traffic Engineering, MPLS based VPN, overlay networks-P2P connections.

Traffic Modeling: Little’s theorem, Need for modeling, Poisson modeling , Non-poisson models, Network performance evaluation.

Network Security and Management:- Principles of cryptography, Authentication, integrity, key distribution and certification , Access control and fire walls, attacks and counter measures, security in many layers. Infrastructure for network management, The internet standard management framework –SMI, MIB, SNMP, Security and administration, ASN.1.

## References:

- Kershenbaum A., “Telecommunications Network Design Algorithms”, Tata McGraw Hill.
- Larry Peterson & Bruce David, “Computer Networks: A System Approach”, Morgan Kaufmann, 2003
- Douskalis B., “IP Telephony: The Integration of Robust VoIP Services”, Pearson Ed. Asia.
- Warland J., Varaiya P., “High-Performance Communication Networks”, Morgan Kaufmann, 1996.
- Stallings W., “High-Speed Networks: TCP/IP and ATM Design Principles”, Prentice Hall, 1998.
- Leon Garcia, Widjaja, “Communication networks”, TMH seventh reprint 2002.
- William Stallings : Network security, essentials- Pearson education Asia publication

## (DEC-II) (B) Automotive Electronics

### Teaching Scheme

Lectures: 3 hrs/week

### Examination Scheme

T1, T2 – 20 marks each, End-Sem Exam -60

### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- CO1: Design the digital control of drives using sensors and Digital Control Systems.
- CO2: Design the starting and braking system for the automobiles.
- CO3: Do research in field of automotive electrical applications.

### Syllabus Contents:

**Introduction:** Microprocessor and micro Computer applications in automobiles; components for engine management system, chassis system, motion control; electronic panel meters.

**Sensors & Actuators:** Different types of Sensors such as oxygen sensors, crank angle position sensors, fuel metering/vehicle speed sensors and detonation sensors, altitude sensors, flow Sensors, throttle position sensors, Solenoids, stepper motors, relays.

**CAN:** Architecture, Data transmission, Layers, Frame formats, applications

**Fuel Injection & Ignition System:** Feedback carburettor system; throttle body injection and multi point fuel injection System; injection system controls; electronic spark timing.

**Engine Control System:** Open loop and closed loop control system; engine cooling and warm-up control; acceleration, deceleration and idle speed control; integrated engine

control system; exhaust emission control engineering; on-board diagnostics; Automotive Electrical: Batteries; starter motor & drive mechanism; D.C. generator and alternator; lighting design; dashboard instruments; horn, warning system and safety devices.

**Comfort & Safety:** Seats, mirrors and sun roofs; central locking and electronic windows; cruise control; in-car multimedia; security; airbag and belt tensioners Electromagnetic Interference Suppression, Electromagnetic compatibility

#### References:

- John B. L Heywood, “Internal Combustion Engine Fundamentals”, Mc-GrawHill Inc.
- Nicolas Navet, “Automotive Embedded Systems Handbook”, edited by, CRC press
- Williams Ribbens, “Understanding Automotive Electronics”, Elsevier Pub.
- Ronald K. Jurgen “Automotive Electronics Handbook”, McGraw Hill Inc
- “BOSCH CAN Specifications Version 2”.

### (DEC-II) (C) Crypto-processors

#### Teaching Scheme

Lectures: 3 hrs/week

#### Examination Scheme

T1, T2 – 20 marks each, End-Sem Exam -60

#### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- CO1: Learn and practice crypto processor based solutions for medium scale enterprises.
- CO2: Deployment of obfuscators as add-on tailor-made modules.
- CO3: Explorations in Internet of Things (IoT) domain.

#### Syllabus Contents:

**Introduction to classical cryptography**, substitution ciphers, Engima machine and Navajo code, Shift and Affine ciphers.

**Tamper Resistance cryptographic Processor**, Homomorphic Crypto Processor design.

Open source cryptographic processor,

**Reconfigurable Cryptographic coprocessor**

Timing channels in cryptography as microarchitectures, Time driven Cache attacks, Branch prediction Attacks.

**Static software based Obfuscation methodologies**, Dynamic obfuscators, design of hardware obfuscator (with Picoblaze) using FPGA.

**References :**

- Tom St. Denis, “Cryptography for developers” , Syngress; 1 edition (January 15, 2007)
- **Rebeiro**, Chester, **Mukhopadhyay**, Debdeep, **Bhattacharya**, Sarani “Timing Channels in cryptography- A Micro-Architectural perspective”, Springer
- **Christian Collberg Jasvir Nagra** “Surreptitious Software”, Addison-Wesley Professional; 1 edition (August 3, 2009)

**Lab for Semester –II**

- The faculty associate with these subjects shall assign laboratory practices to the students, minimum FOUR per course.
- The laboratory practices shall encompass implementation/ deployment of the course work in terms of the hardware setup, algorithm development and programming assignment.
- The student shall submit such assignment in the hard/soft copy format to the concerned faculty for further evaluation.

**(LC) DSP Architecture Lab****Teaching Scheme**

Practical: 2 Hrs / Week

**Examination Scheme**

Term work/Practical: 100 Marks

**Course outcomes:**

- Understand the basic DSP working tools for the TI6000 Platform
- Familiarization with the basics of C6713 processor VLIW Architecture, Assembly language Instruction set, and the register usage of the C runtime model using Code Composer Studio Version 5 in Windows 7 platform.

**Phase I: Preliminaries of Code Composer Studio and DSK6713 Kit (Seven Experiments)**

The experiments in this phase are oriented to familiarize students with the basics of C6713 processor interface through Code Composer Studio, Simulation and DSK6713 kit exposure.

- Expt. 1 Installation of the Code Composer Studio Tool
- Expt. 2 Creating a new project and addition of include files to the project
- Expt. 3 Compilation and Execution of C programs and checking the results using the Simulator mode of CCS
- Expt. 4 Study and familiarity with the DSK 6713 kit
- Expt. 5 On-Line diagnostic for the DSP 6713 kit
- Expt. 6 Practice C programming in Simulator mode for image processing techniques like Median filters
- Expt. 7 Practice C programming in Simulator mode for Fuzzy logic operations

**Phase II: TMS320C6713 Architecture, Instruction Set Studies (Ten Experiments)**

The experiments in this phase are organized as C6713 Processor VLIW architecture internals, Assembly Language Programming, Application Programming using C Language, Use of Pseudo Instructions: Impact of NOP instructions and IDLE instructions, Timing Analysis for C6713 processor using on chip timer registers and DSK Board /Kit. At least one experiment on each of these modules.

- (A) DSKC6713 Kit
- (B) Assembly Language Programming: Assembler Directives like .set . data , .equ and Simply Assembly programming practice.
- (C) Application Programming using C Language: Use of Code Compiler Studio Version 5 with C Compiler and Assembly routines, setting of paths, include, linker options, disassembly, verification of variables, registers and memory locations
- (D) Use of Pseudo Instructions: Impact of NOP instructions and IDLE instructions.
- (E) Timing Analysis for C6713 processor using on chip timer registers.
- (F) DSK Board /Kit

- Expt 1(a) : Functional unit assignments:
- Expt 1(b) : Verify the contents of core data path registers (DSP processor set in Little endian mode)?
- Expt 2: Computation of two complex number multiplication using assembly code. Assume the complex numbers  $C1=3+j4$  and  $C2=6+j8$
- Expt 3: Write an assembly code to compute Euclidian distance between two points (3,4) and (6,8). Write a C program to use this assembly code as a function.
- Expt 4: Write an assembly function for *min*-fuzzy operation and use it in a C-program code to compute a fuzzy relation for the fuzzy sets.
- Expt 5: Explore the assembly code for NOP / IDLE effectiveness.
- Expt 6: Estimate the MAC per second for the TMS320C6713 processor (Text book section 15.3.3, 15.3.4).
- Expt 7: Sine wave Generation and playing audio note through Codec.
- Expt 8-10: Selected traditional DSP algorithms and implementation on DSP 6713 kit (actual details to be changed from semester to semester)

### **Phase III: Mini Project (s) using TMS320C6713 (Possibly with LabView also)**

#### **(LC) Real Time Operating Systems Lab**

##### **Teaching Scheme**

Practical: 2 Hrs / Week

##### **Examination Scheme**

Term work/Practical: 100 Marks

##### **Course outcomes:**

- To understand the features and structures of practical implementations and how application areas impact on real-time operating system facilities.

##### **List of Practical:**

1. Controlling of peripherals without using  $\mu$ C/OS -II services.
2. Study of Task creation using OSTaskCreate()
3. Study of Task creation using OSTaskCreateExt()
4. Exploring multitasking features of  $\mu$ C/OS -II.
5. Study of Semaphore Service of  $\mu$ C/OS -II.
6. Study of Mutex Service of  $\mu$ C/OS -II.
7. Exploring Mailbox management Services of  $\mu$ C/OS -II.
8. Exploring Message Queue Services of  $\mu$ C/OS -II.
9. Real Time Application Development using  $\mu$ C/OS -II services.

#### **(LC) Digital CMOS VLSI Design Lab**

##### **Teaching Scheme**

Practical: 2 Hrs / Week

##### **Examination Scheme**

Term work/Practical: 100 Marks

##### **Course Outcomes (COs)**

At the end of this course students will demonstrate the ability to

- Understand Digital Circuit design using CMOS.
- Build blocks of a system to solve engineering problems.
- Use EDA tools like Cadence, Mentor Graphics and other open source software tools like NGSPICE through lab exercises.

##### **List of assignments:**

1. SPICE simulation of basic analog circuits.
2. Analog Circuit simulation using Cadence tools
3. Verification of layouts (DRC, LVS)
4. Back annotation

## (MLC) Intellectual Property Rights

### Teaching Scheme

Lectures: 3 hrs/week

### Examination Scheme

Marks: 100

### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

CO1: Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.

CO2: Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.

CO3: Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

### Syllabus Contents:

- UNIT I** (6)  
1. Introduction: Nature of Intellectual Property: Patents, Designs, Trademarks and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development.
- UNIT II** (4)  
International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.
- UNIT III** (4)  
Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.
- UNIT IV** (4)  
New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Softwares etc. Traditional knowledge Case Studies, IPR and IITs.
- UNIT V** (4)  
Registered and unregistered trademarks, design, concept, idea patenting.

**References:**

- Halbert, “Resisting Intellectual Property”, Taylor & Francis Ltd ,2007
- Mayall , “Industrial Design”, Mc Graw Hill
- Niebel , “Product Design”, Mc Graw Hill
- Asimov , “Introduction to Design”, Prentice Hall
- Robert P. Merges, Peter S. Menell, Mark A. Lemley, “ Intellectual Property in New Technological Age”.
- T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand.

**(LLC) Liberal Learning Course****Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

**CO1:** Exhibit self learning capabilities and its use in effective communication.

**CO2:** Inculcate impact of various areas to relate with society at large.

**Syllabus Contents:**

Identification of topic and resources, scope, and synthesize viewpoints for the areas such as performing arts, social sciences, business, philosophy, Agriculture sports and athletics, Fine Arts Medicine and Health Linguistics, defense studies and education.

## Semester-III and Semester-IV

### (Dissertation) Dissertation Phase – I and II

#### Teaching Scheme

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#### Examination Scheme

Marks: 100 each for phase I and II

#### Dissertation Phase – I

##### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- CO1: Pursue detailed Literature Survey.
- CO2: Define Problem and Objectives.
- CO3: Design and conduct basic experimentation for proof of concept.

#### Dissertation Phase – II

##### Course Outcomes:

At the end of the course, students will demonstrate the ability to:

- CO1: Carry forward the experimentation towards final conclusions.
- CO2: Produce a prototype for verification and testing.
- CO3: Prepare documentation followed by publications.

#### Guidelines:

As per the AICTE directives, the dissertation is a yearlong activity, to be carried out and evaluated in two phases i.e. Phase – I: July to December and Phase – II: January to June.

The dissertation may be carried out preferably in-house i.e. department's laboratories and centers OR in industry allotted through department's T & P coordinator.

After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.

Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit

the proposal within a month from the date of registration.

**Phase – I deliverables:** A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.

**Phase – I evaluation:** A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend repeating the phase-I work.

During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences OR IP/Patents.

**Phase – II deliverables:** A dissertation report as per the specified format, developed system in the form of hardware and/or software, A record of continuous progress.

**Phase – II evaluation:** Guide along with appointed external examiner shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend for extension or repeating the work.