College of Engineering, Pune
END SEMESTER EXAM Nov 2011
S.Y. B.Tech (Electronics and Telecommunication)
(ET 202)- Digital Electronics and HDL

Day & Date- /11 /2011 Max.Marks- 50

Timing- Duration – 3 Hrs

Instructions:
1. All questions are compulsory.
2. Neat Diagrams must be drawn wherever necessary.
3. Assume suitable data, if necessary.
4. Figures to the right indicate full marks

Q. 1	A	1. What is a gray code for decimal number 20 2. Perform BCD subtraction (87-29)	05
	B	List the devices used for generating clock signal. Explain with diagram how a level triggered clock is converted into edge triggered clock	05
Q. 2		A sequential clock has one external input x and three states as A, B and C. As long as x is 0, the circuit alternates between states A and B. If x becomes 1(either in state A or B), the circuit goes to state C and remains in state C as long as x continues to be 1. The circuit returns to state A if input becomes 0 and repeats. Assume the state assignments as A=00, B=01 and C=10 1. Draw the state diagram and state table 2. Design the circuit using JK FF 3. Draw the ASM chart	10
Q. 3	A	Write a VHDL code for 4:1 MUX using all 2:1 MUX	05
		OR	
	A	Write VHDL code for 2 bit adder using full adders	05
	B	Write VHDL code for T FF using behavioral model with synchronous reset	05
Q. 4	A	Write short notes on (any two) a. Flow of VHDL b. Set up and Hold time c. Moore and Mealy m/c	05
	B	Explain delays in VHDL	05
Q. 5		Define the terms (any five) 1. Noise margin 2. Totem pole configuration 3. Source and sink current 4. 4. Low schottky TTL device 5. 5. FAN IN and FAN OUT 6. I/P and O/P profile of CMOS	10