College of Engineering, Pune

(SY B Tech)- (Electronics and Telecommunication)

(EC-206)- (Integrated Circuits and Applications)

Date- 09/05/2012
Academic Year: 2011- 12

Timing: 3 hrs
Max. Marks: 50

Spring Semester

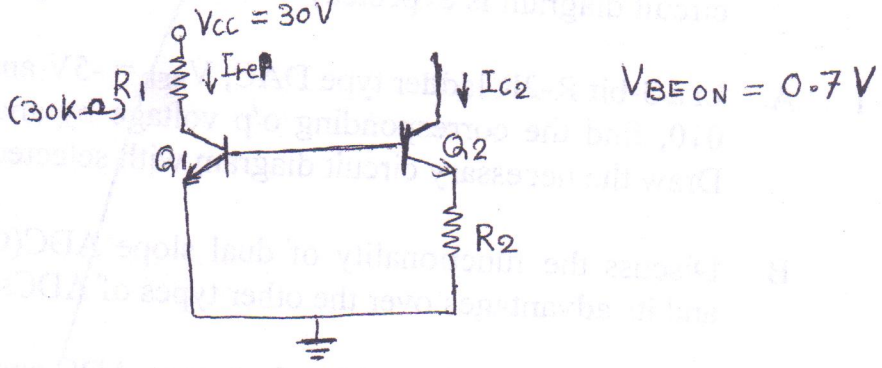
Instructions:

1. **Sub-question A from each question is compulsory and solve any one from B and C.**
2. Assume suitable data wherever necessary.
3. Figures to right indicate full marks.

Q.1 A. With given specifications, design a waveform generator using IC 8038 for Vcc = 10V: Output frequency = 2 KHz, Duty cycle = 50%. Draw corresponding waveforms of all three outputs. Discuss the effect of V_I on output frequency with appropriate reason. 05

B. Design a Schmitt trigger for V_{LTP} = -2 V, V_{UTP} = 5V. Assume $\pm V_{SAT} = \pm 10$ V. Draw the circuit diagram and waveforms. 05

C. Design the Widlar current source with npn transistor that produces 10μA output current. 05



Q. 2 A. Design a phase locked loop with IC 565 for f_o = 2 KHz. Find the values of R_1, C_1 and C_2 for the capture range of 30% of lock range. Assume $\pm V_{cc} = \pm 10$ V. 05

B. With appropriate block diagram explain PLL as frequency multiplier. 05

C. What are different types of phase detectors used in PLL (diagrams are expected)? Write the advantages and disadvantages of all phase detectors. 05

Q. 3 A. Design an astable multivibrator (IC 741 based) for the duty cycle of 70%. Draw the circuit diagram and necessary waveforms. 05

B. 1) Can IC 555 based astable multivibrator have 50% duty cycle? If YES write the solution. 05
2) Discuss the log and antilog amplifier for voltage multiplier. State their limitations.

C. Discuss any one diagram of full wave precision rectifier with circuit diagram and waveforms. 05

Q.4 A. If the amplitude of output of the multivibrator designed in Q. 3A is to be varied from 1V to 30V what changes are needed? Design the modified circuit. 05

B. What is peak detector? Explain with diagram and waveforms. 05

C. Starting with theoretical differentiator state its limitations and how those can be overcome in practical differentiator. (waveforms and circuit diagram is expected) 05

Q. 1 A. In a 3-bit R-2R ladder type DAC, V_{REF} = -5V and data i/p is binary 010, find the corresponding o/p voltage by analyzing the circuit. Draw the necessary circuit diagram with selected components. 05

B. Discuss the functionality of dual slope ADC(Graph is expected) and its advantages over the other types of ADCs. 05

C. Define the following with reference to ADC and DAC 05
i) Resolution ii) Linearity iii) Accuracy iv) Settling time
v) Stability