MISNO:

COLLEGE OF ENGINEERING, PUNE

(An Autonomous Institute of Government of Maharashtra.)

SHIVAJI NAGAR, PUNE - 411 005

End Semester Examination

(CT-202) Digital Systems

Course: B.Tech   Branch:I.T- Comp Engg.
Semester - III
Year:2014-15   Max. Marks: 60
Duration:3 hrs   Time :10:00-1:00 p.m   Date: 26/11/2014

Instructions:

1. Figures to the right indicate the full marks.
2. Mobile phones and programmable calculators are strictly prohibited.
3. Writing anything on question paper is not allowed.
4. Exchange/Sharing of anythings like stationery, calculator is not allowed.
5. Assume suitable data if necessary.
6. Write your MIS Number on Question Paper
7. Write answers for each section in separate answer sheets provided.

Q1 a   Explain in details what do you understand by PLD's. Write short note on PLA   5 m

A combinational circuit is defined by the function-

$F1(A,B,C)=\Sigma(3,5,6,7)$

$F2(A,B,C)=\Sigma(0,2,4,7)$

Implement the circuit with a PLA having 3 inputs, 4 product terms, and two outputs.

Q1 b   Explain with logic diagram clocked RS Flip-Flop using four NAND gates and   5 m
D- flip-flop with AND and NOR gates.

OR

Explain in detail Static RAM memory cell.
                                                                                        5 m
Draw timing diagram for WRITE cycle for static RAM cell.

Q2   Use the QM Method for minimization and find expression for following   10 m
        function F(A,B,C,D) = $\sum$M(0,1,2,3,5,7,8,9,11,14)

Q3   Explain the SISO Register design for input data string 1010 with the neat logic   10 m
        diagram. Draw corresponding waveforms for its functioning.

                                    Section B

Q4   Design a synchronous counter that counts 000,010,101,110,000,010.........   10 m
        Ensure that the unused states of 001,011,100 and 111 go to 000 on next clock
        pulse.

        Use JK-flipflops for designing the counter.

        What will be the modulus of the counter?

        How will the counter look like if unused states are to be considered as don't care
        conditions.

Q5   What do you understand by Shift register counter. Describe 4-bit Circulating   10 m
        counter in detail with waveforms. Determine the number of flipflops required to
        construct-

        a.Mod-10 Ring counter

        b.Mod-10Johnson counter

        c. State the count sequence in both cases (a) and (b)

Q6   Draw ASM chart , state table and state diagram for synchronous circuit. The   10 m
        circuit has control input 'C' clock and outputs as x,y,z.

        If C=1,on every clock rising edge the code on output x,y & z changes from
              000--->010--->100--->110--->000 and repeats.

        If C=0 circuit holds present state.

        Write short note on ASM.

                                       OR

Q6   What is VHDL ? Write VHDL code for SR latch using NAND gates.   10 m