COLLEGE OF ENGINEERING, PUNE

(An Autonomous Institute of Govt. of Maharashtra) Comp.

END-SEM EXAM

(CT301) Computer Organisation

Program: T.Y.B. Tech (Computer Engineering)

Year: 20012-13 Semester I Date: 24/11/2012

Duration: 3 hrs Max. Marks: 100

Instructions:

1. Answer all questions.
2. Figures to right indicate full marks
3. Draw neat figures wherever required.
4. Assume suitable data, if necessary.

Marks

Q.1 a Consider the following part of code:

```
int X = 0, Y = 0;  // The compiler puts X in R1 and Y in R2.
int i;  // The compiler puts i in R3.
int A[4096];  // A is in memory at address 0x10000

for (i=0; i<1024; i++)
{
X += A[i];
}

for (i=0; i<1024; i++)
{
Y+= A[i+2048];
}
```

Answer the following:

(I)Assume that the system has 8KB direct-mapped data cache with16-bytes per block. Also assume that the integers are 32-bits and initially the cache is empty.
What is the series of data cache hits and misses for this part of code? **4**

(II)Assume that the system has 8KB two-way set associative data cache with 8-bytes per block and having LRU replacement policy. Also assume that the integers are 32-bits and initially the cache is empty.
What is the series of data cache hits and misses for the same part of code? **4**

b What are the various levels of RAID? **10**

P.T.O.

Q.2		Show the organization of a single bus CPU with eight general purpose registers R0, R1, ...R7 and the required dedicated registers & other functional blocks. Indicate the major control signals therein. What are the control signals to be generated therein for executing the following instruction to store the result in memory: AND [R5], R3?	**16**
Q.3	a	Give the schematic of floating point addition-subtraction unit. How is the sign of the result finalized?	**10**
	b	As per the above logic, perform (**X** + **Y**), if X & Y are the floating point numbers in IEEE754 single precision format **X** = 41904000h & **Y**= C0A40000h	**8**
Q.4	a	Give the lower 1MB memory map of x86 based computing machine.	**8**
	b	Explain the loading of Disk Operating System along with the memory map.	**8**
	OR		
	b	What are the architectural features of NDP 8087?	**8**
Q.5	a	What is lookahead carry in four bit addition?	**6**
	b	Explain the translation of virtual address to physical address, if the virtual address space is 2MB and the physical address space is 64KB, with page size of 4KB What is thrashing in demand paging?	**10**
	OR		
	b	Explain IBM PC Colour Graphics Adapter	**10**
Q.6	a	What are the features of RISC machine?	**6**
	b	Describe Register set supporting 8 windows in SPARC.	**10**
	OR		
	b	Describe the MESI protocol for cache consistency.	**10**