COLLEGE OF ENGINEERING, PUNE
(An Autonomous Institute of Govt. of Maharashtra)
END-SEM EXAM
(CT-318) Microprocessors and Microcontrollers
Program: T.Y.B. Tech (Computer Engineering)

Year: 2012-13   Semester II   Date: 2/05/2013

Duration: 3 hrs   Max. Marks: 100

Instructions:
1. Answer all questions.
2. Figures to right indicate full marks
3. Draw neat figures wherever required.
4. Assume necessary data, if needed.

			Marks
Q.1	**a**	Define the descriptor for referring the data segment of 4MB available from 00800000 onwards in IA-32 Processor based system. Point out the attributes of the same.	8
	b	What are the conforming & non conforming code segments? Are there any restrictions in accessing them?	5
	c	What are expand up stack and expand down stack?	5
Q.2	**a**	Explain CALL GATE descriptor and when it's needed. Show neatly the flow to reach desired code area using CALL GATE, including appropriate stack references. What are the restrictions therein?	12
	OR		

	a	Explain the following w.r.t. 8031/8051
		  i) Register banks and bit addressable RAM
		  ii) Serial communication facility
		  iii) Interrupt handling facility
			12

	b	Answer the following
		  i) What is the purpose of I/O bit map and where is it located?
		  ii) What is the difference in TRAP and FAULT?
			6

Q.3	**a**	What is the role of LDTR register? What are the possible ways to get it initialized?	8
	b	What is the action of IA-32 CPU for executing following instruction? LTR memory	8

P.T.O.

| Q.4 | a | How is the provision made for MMX registers in IA-32 processor? What is the role of EMMS instruction? | 8 |

| | b | Explain the following with respect to Streaming SIMD Extensions (SSE) execution environment | 8 |

i) Flush to Zero (FZ) mode & Denormals Are Zeros (DAZ) mode
ii) SIMD computation and scalar computation

| Q.5 | a | What is the structure of Virtual 8086 Task? Explain the entering and leaving Virtual 8086 mode | 10 |

OR

| | a | Explain the System management mode in Pentium? | 10 |

| | b | How does IA-32 Processor support for Intel HyperThreading Technology? Describe system schematic supporting Intel quad-core technology & Intel HyperThreading Technology in Intel Core i7 processors. | 6 |

| Q.6 | a | What are various memory types for caching? What are the various Memory Type Range Registers (MTRRs)? | 10 |

| | b | Answer the following | 6 |

i) What is the need of null descriptor in GDT?
ii) How is paging advantageous in V8086 tasks?