College of Engineering, Pune
End Semester Exam – May 2012
First Year M.Tech. (Electronics – Digital Systems and VLSI & ES)
(ET)- (Advanced Embedded Architecture)

Day & Date- Friday, 11/05/2012 Time: - 9.00 am to 12.00 noon
Maximum Marks: 100 Duration – 3 Hrs.

Instructions:

1) All the major questions are compulsory. Regarding sub-questions follow the instructions specified at the beginning of each question.
2) Neat Diagrams must be drawn wherever necessary.
3) Assume suitable data, if necessary.
4) Figures to the right indicate full marks.

Q. 1 Attempt any FIVE of the following. (20)

A. CS, DS, ES and SS registers are in the IA-32 architecture. How many bits are these registers? Explain the formats of these registers in Real and Protected modes. Where do these register point in these two modes? (04)

B. GDTR is 48 bits and has base register & limit field, and can access GDT of 64 KB anywhere in the 4 GB space. The LDTR is only 16 bits. How can it access the LDT which can be of the same size of GDT? (02)

C. What is difference between Call Gate, Task Gate and Interrupt Gate? How does i386 identify which Gate it is? Indicate there fields. (04)

D. IA-32 architecture has an address space of 4 GB. Limit field in the segment descriptors is only 20 bits. How can segments greater than 1 MB be created? (02)

E. Draw neat labeled diagram of the following. (04)

i. System Block diagram of Intel ATOM processor E6xx series.

OR

ii. Components of Intel ATOM processor E6xx series.

F. What is difference between P-states and C-states in power management of processor chips? Can you have combination of P-states with any of the C- states? (04)

G. How many cache units are there in ATOM processor as seen in micro-architecture and their size? (02)

H. Draw flow-chart of software activity to enable and disable protected mode in i386 processor. (04)

Q. 2 Answer any ONE of the following. (16)

A. How is memory segmentation achieved in protected mode of IA-32? Show how logical address is converted into linear and physical address? Explain this with a neat labeled diagram when PE bit = 0 and PE bit = 1 in CR0 register.

B. How many privilege levels are there in the IA – 32 architecture and where are they defined? Explain the methods of changing privilege level of code from lower to higher.

Q. 3 Answer any ONE of the following. (16)

A. Explain the components of the ATOM processor and the functions of front-end, integer and floating point execution and memory execution clusters. Clearly show the stages of integer and floating point pipelines.

B. Explain the principle of block and interleaved multithreading and state limitations of both. Discuss how hyper-threading is implemented in the Intel architectures and how does it improve the performance?

Q.4 Answer any TWO of the following.

A. What are the primary functions of local and external Advanced Programmable Interrupt Controller (APIC)? Draw and explain block diagram showing the connection between local and external APIC in multiprocessor system. How are the inter-processor interrupt (IPI) messages are generated by local APIC? (08)

B. What are the common blocks of typical PC platform and its role? Explain evolution and need from 3 chip to 2 chip solutions in recent IA platforms. (08)

C. Bring out the differences between the exception processing by the 80386 processor in real and protected mode. Comment on the state of interrupt vector table during switching from real to protected mode and back. (08)

D. Explain the tasks performed as part of the BIOS boot sequence for a typical IA platform. Elaborate on POST, setup and runtime sections. (08)

Q.5 Answer any ONE of the following. (16)

A. What is Advanced Configuration and Power Interface (ACPI)? Explain the power states of the ACPI specifications. What is the expression for the total power consumption?

B. Explain the CPU C-states power saving modes. Indicate clearly the sequence of the states and support provided by the CPU and OS.

Q.6 Answer any ONE of the following. (16)

A. With the number of vehicles growing day by day, there has been an increase in road accidents, traffic congestion and pollution. Automated Guided Vehicles (AGV) ensures improved safety, more fuel economy, and efficient traffic flow. Auto Drive is a prototype of an AGV that can be used as an autonomous taxi in college campuses or technology parks. It uses a host of different sensors and actuators, along with GPS receivers, to navigate around the campus based on a set of user defined waypoints. Beside GPS, Auto Drive uses a camera for lane detection, sonar and infrared range finders for obstacle sensing, and the motor's optical encoders for acquiring positional information.

1. According to you, what are the challenges in designing and implementing the Auto Drive system?

2. Identify, draw and explain functional block diagram for the Auto Drive system.
3. Analyze the design and bring out features and limitations of the Auto Drive system.

B. A Cable Modem front-end architecture and software was originally designed and developed to run on an ARM 4-core processor. The design has three distinct types of packets – up-stream, down-stream and control packets which are time critical. Control packets specify the time of up-stream packet a node can deliver. Up-streaming and down-streaming can be assigned to different processor cores. The project is to be implemented on the ATOM processor. Indicate and explain the steps in migrating software to the ATOM processor.

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COLLEGE OF ENGINEERING PUNE

END SEMESTER EXAMINATION 2011-2012

MICROELECTRONICS

Program: F.Y.M.Tech (DS) Time: 09.00 am – 12.00 noon

Date: 08/05/2012 Max Marks: 50

Instructions:

1. All questions are compulsory.
2. Draw appropriate circuit diagram and waveform wherever necessary.
3. Numbers in square brackets reflects marks.

Q1. State True or False [10]

a) The load capacitance of a static CMOS gate affects its VTC.

b) The delay of a static inverter is increased if (W/L)p / (W/L)n is equal to $\mu n/\mu p$.

c) A NOR based ROM structure is typically faster and compact than a NAND based one.

d) The speed of a ring oscillator can continuously be improved by exponentially decreasing the W/L ratio of the inverters.

e) rc delays of the interconnect network should be considered only when t_{pRC} is comparable or larger than the t_{pgate} of the driving gate.

f) rc delays should only be considered when the rise (fall) time at the line input is larger than RC, the rise (fall) time of the line.

g) Switching Threshold V_M is relatively sensitive to variations in the device ratio.

h) A CMOS inverter can be used as an analog amplifier in its transition region.

i) The impact of input slope decreases with reduced supply voltage (for fixed thresholds).

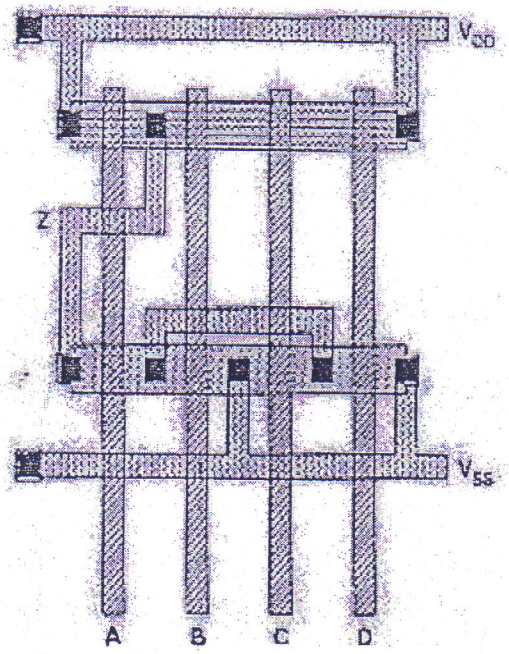
j) In contrast to complementary CMOS, the NOR structure is the preferred topology for pseudo-NMOS.

Q2. Draw the stick diagram for a CMOS gate computing the following logic functions. [5]

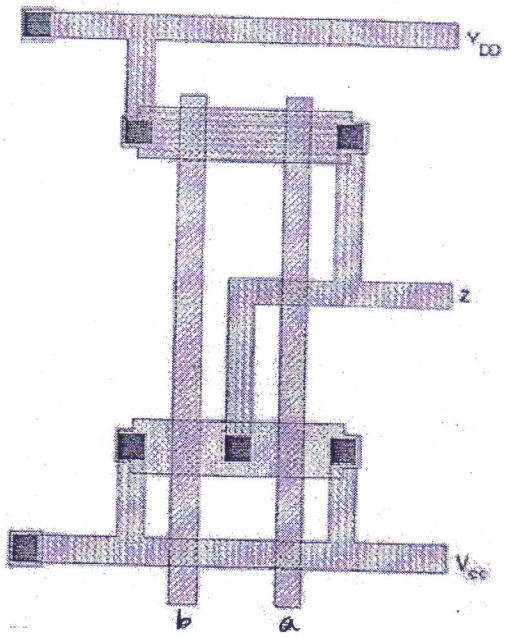
a) $Y = (A \cdot B) + C$

b) $Y = ((A + B + C) \cdot D)'$

Q3. From the stick diagram given below, identify the circuit and draw its transistor level schematic. [5]

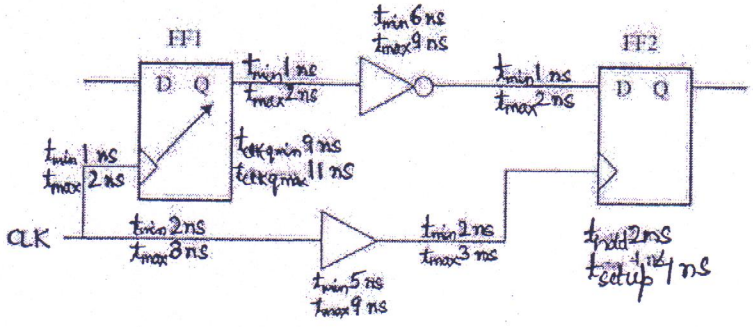


a)



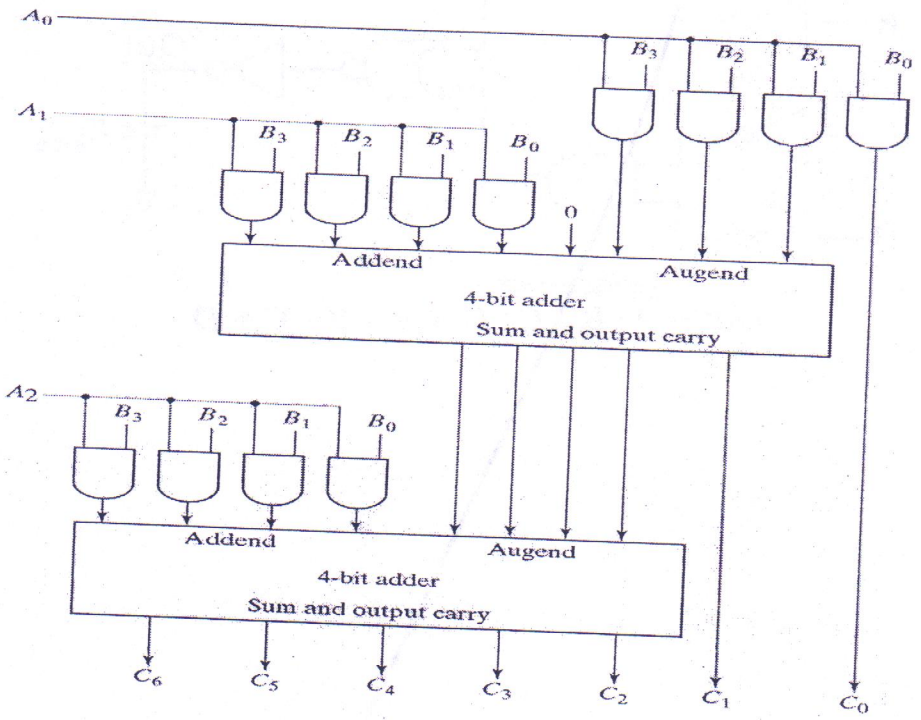
b)

Q4. In the following circuit find whether there is any set-up or hold violation. Justify. [10]



Q5. The following circuit realizes a combinational circuit design. Identify the circuit. Justify with proper reasons.

[10]



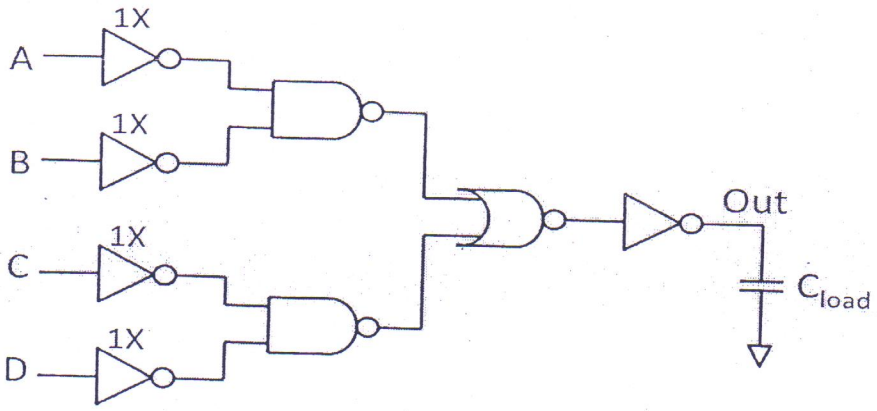
Q6. Following schematic implements the logic equation of (A+B+C+D). The four inverters connected to inputs are minimum sized.

[10]

a) If C_{load} is $25xC_{gmin}$, where C_{gmin} is the gate capacitance of a minimum-size inverter. Size the NAND, NOR and INV gates to minimize the propagation delay from input to output.

b) Repeat part (a) if C_{load} is $1xC_{gmin}$.

c)Can you design another circuit that implements the same logic but has shorter propagation delay for the case of $C_{load} = 1xC_{gmin}$? The four input inverters come from the I/O interface design. They can neither be replaced nor be resized.



$$Out = \overline{A \cdot B + C \cdot D} = A + B + C + D$$