College of Engineering, Pune- 5

Department of Electronics and Telecommunication Engineering

END Semester Examination

Subject- Embedded Software & Real Time Operating System (ES&RTOS)
Max Marks- 50 **Academic year-2011-12**
Class- M.Tech (VLSI & Embedded / Digital Systems) **Date:**

Special Instructions if any
1. **Question No.01, 06 and 07 are compulsory.**
2. **Figures to indicate full marks**

Q.1 a) Explain memory management technique in RTOS - (04)

b) How memory management is done in µC/OS – II? - (06)

Q.2 a) What is ECB? Illustrate typical usage of ECB. - (06)

b) Explain OSEventTaskWait ( ) and OSEventTO ( ) – (04)

OR

Q.3 a) Compare and contrast message mailbox and queue - (05)

b) Can we use mailbox instead of OSTimeDly ( )? If yes, justify - (05)

Q.4 a) Explain data structure used in message queue. - (04)

b) What is difference between OSQPost () and OSQPostFront ()? Explain example usage of OSQPostFront () - (06)

OR

Q.5 a) What are considerations for interrupts under µC/OS – II? - (05)

b) Explain the highlight the importance of OS_Config.h -(05)

Q.6 a) What is porting? Discuss requirements of a processor to run µC/OS – II. - (05)

b) Explain general guidelines to port µC/OS – II on given hardware - (05)

Q.7 Construct an application that utilizes at least 04 µC/OS – II services. Justify the real time component in selected application and role of µC/OS – II. – (10)

College of Engineering, Pune
END SEMESTER EXAMINATION-May 2012
F.Y. M.Tech (VLSI)
Reconfigurable Computing

Date- 08 /05/2012 Max.Marks- 50
Timing- 9am -12noon Duration – 3 Hrs

Instructions:
1. All questions are compulsory.
2. Neat Diagrams must be drawn wherever necessary.
3. Assume suitable data, if necessary.
4. Figures to the right indicate full marks

Q. 1		Write a VHDL code to find out the minimum number and maximum number from an array of 10 numbers also find their respective position	10
Q. 2	A	What is coarse grained reconfigurable device? Classify them and explain any one device	05
	B	List out the different reconfiguration modes of FPGA and explain the one which is most widely used	05
Q. 3		Differentiate the following(any two)	10
	A	Two level decomposition vs Multilevel decomposition	
	B	Run time configuration vs Compile time configuration	
	C	Synthesis vs Simulation	
Q. 4		Write short notes on (any two)	10
	A	System on programmable chip	
	B	Design for testability	
	C	Chortle algorithm for LUT mapping	
Q. 5		Solve any two	10
	A	Which are the criteria you will look for choosing a FPGA	
	B	Explain the clocking and timing issues related to digital systems	
	C	Design a 16 bit adder with 4ns delay, we have 8 bit adder and a mux with 3ns and 1ns delay resp. You can use any numbers of 8 bit adder	

COLLEGE OF ENGINEERING, PUNE

(An autonomous institute of Government of Maharashtra)

END SEMESTER EXAMINATION 2011-12

Subject: - System-on-Chip

Program: - M.Tech-I (VLSI and Embedded Systems) **Date: 11/05/2012**

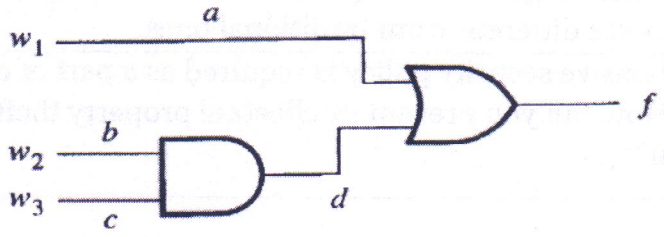
Duration: - 3.00 Hrs **Max. Marks:** - 50

Instructions:-

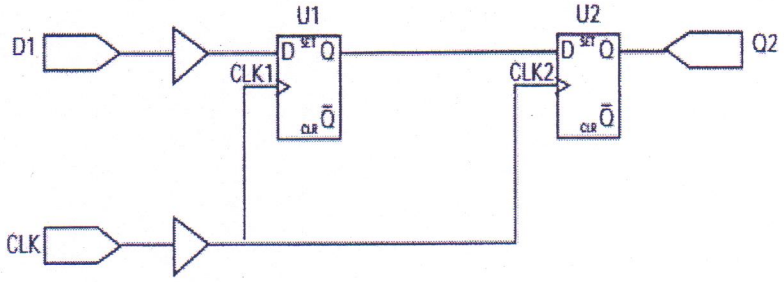
1. Attempt any **FIVE** questions.
2. Do not carry Cell phone & programmable calculator.
3. Figures to the right indicate full marks.
4. Draw neat diagrams wherever required.
5. Assume suitable data if necessary.
6. **Answers to the points are desirable.**

Q.1	**A)**	Why verification component is necessary in system design using HDL? How conventionally formal verification is carried out? What are their merits & demerits? How automate methodologies address some of the challenges exist in conventional techniques of formal verification? In verification language "e", How comment and code is distinguished as compared with language "C".	**10**

Q.2	**A)**	Why several architectures are developed (necessary)? List out main groups of architectures. Explain with a suitable example, how instruction level parallelism optimize the hardware utilization.	**5**
	B)	What are the three main parts consist in a FPGA. Justify FPGA as a programmable device. What technology/ies are in use to program FPGA several times? Explain with a suitable diagram any one technology used in FPGA.	**5**

Q.3	**A)**	Why testing of logic circuit is essential? List out various testing techniques used to verify the functionality of the designed logic circuit.	**5**
	B)	For a given three input circuit, determine the smallest test set with considering fault model in which each wire can be stuck either at 0 or 1. 	**5**

Q.4	**A)**	Represent the following given expression by a network graph. $F = ae+af+ag+bce+bcf+bcg+bde+bdf+bdg$ Convert the same expression as a multilevel circuit and Calculate the no. of transistors required in either case.	**5**
	B)	Consider a cell library consisting of INV,NAND2,NOR2,AOI21,AOI22,OAI21 and OAI22 i) ASSUMING AN INVERTER ,AND ,TWO INPUT NOR as base functions, Obtain the pattern graphs for all the cells in the library . ii) Repeat part I assuming an inverter and two input NAND as base functions.	**5**

Q.5	**A)**	Find co-kernels and kernels of each of these given functions & tabulate the Complete Co-kernel-Cube Matrix for the given set of Boolean functions (nodes in a network) as used in technology independent synthesis. $F = af + bf + ag + cg + ade + bde + cde$ $G = af + bf + ace + bce$ $H = ade + cde$	**5**
	B)	What clock skew causes? How it can be prevented? For the given simple circuit. Draw the waveform at various points such as at clk, clk1, clk2, with sample waveform at D1, Q1, and at Q2 points to indicate the effect of clock skew. In modern Semiconductors/FPGAs how it has been compensated? 	**5**

Q.6	**A)**	What benefits are obtained in integrating a large digital system into a single integrated circuit? Are there any drawbacks associated with SOC imposed on design engineer? If any discuss. In what respect New SOC methodologies are different from traditional ones.	**5**
	B)	Why comprehensive security policy is required as a part of corporate governance? How can you prevent intellectual property theft in case of system design?	**5**